

15.6" Grant 1.0 / 17.3" Bogart 1.0
Intel Huron River Sandy Bridge 32nm SV PGA988B i3, i5 DC 35W/ i7 QC 45W

15.6",17.3" GDDR5 x 4(1GB), Seymour XT M2(29x29) 15W Muxless Hybrid Switchable
15.6",17.3" GDDR5 x8(1GB,2GB), Whistler XT M2(29x29) 35W Muxless Hybrid Switchable

POWER

Adapter-in Jack w/Smart pin
DC in Conn
Battery Conn
CHARGER: +VCHGR

3.3VSTBY / 5VSTBY 41

DDR3: 1.5V / 0.75VS_DDR_VTT
DDR_VTTR 46

CPU CORE
45W/35W : CPU_CORE 42, 43

CPU PLL : 1.8VS LDO 47

1.1V LDO : USB3.0 37

UMA in CPU: VGFX_CORE 43

CPU IO: 1.05VS_VCCIO 44
== PCH CORE: 1.05VS

CPU IO(0.9V~0.8V): VCCSA 45

POWER GOOD 38

RUN POWER /SUS POWER 39

POWER GOOD 39

5VSTBY----> 5VS 39

1.5V ----> 1.5VS == 1.5VS_CPUVDDQ39

3.3VSTBY----> 3.3VS 39

3.3VSTBY----> 3.3VSTBY_PCH 39

3.3VSTBY----> 3.3V_LAN 39

POWER of
Discrete VGA

VGA_CORE 57
35W /25W / 15W: VGA_CORE

LDO: VGA_1.0VS 56

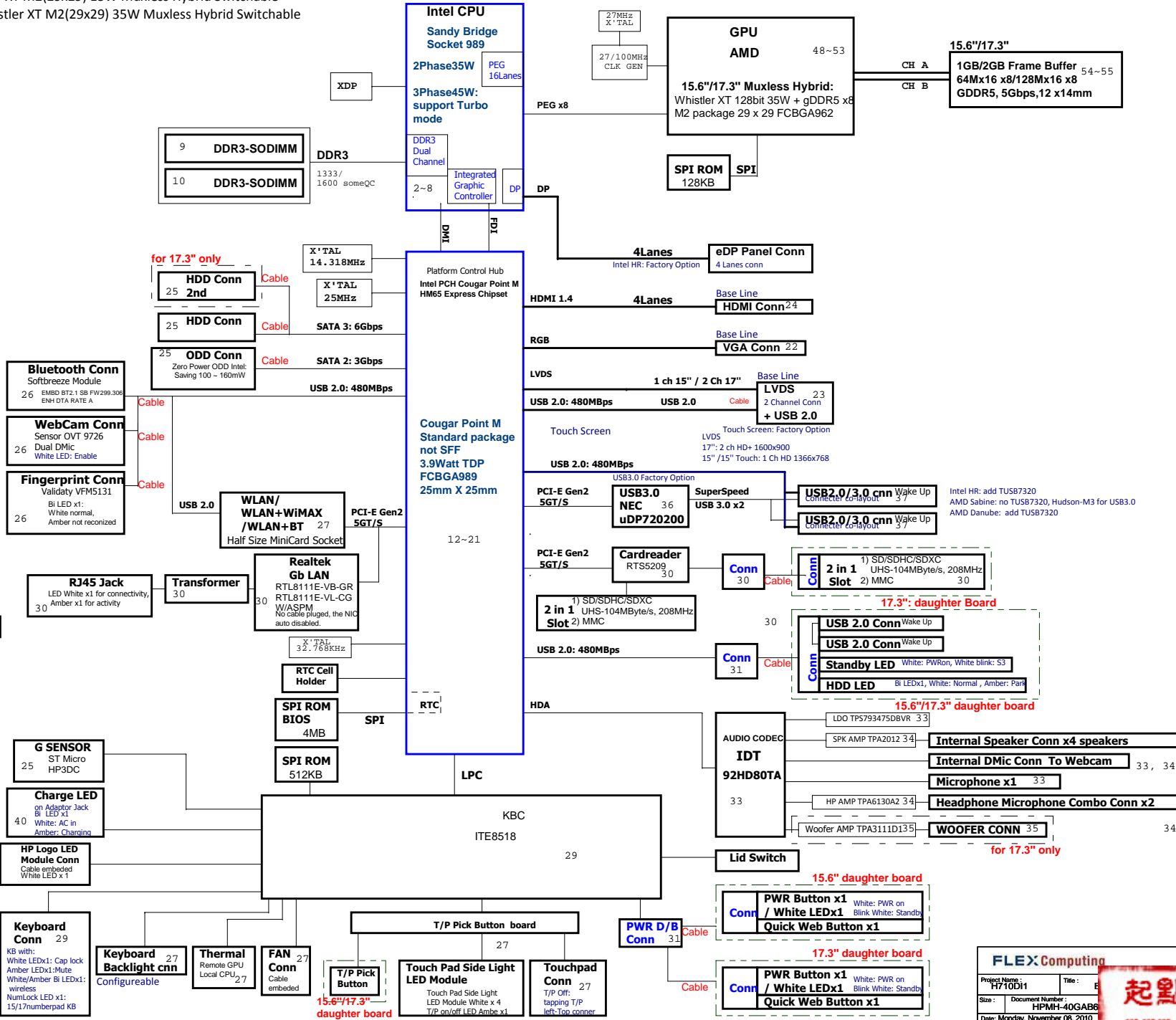
LDO: VGA_1.8VS 56

3.3VS == VGA_3.3VS 56

1.5V ----> VGA_1.5VS 56

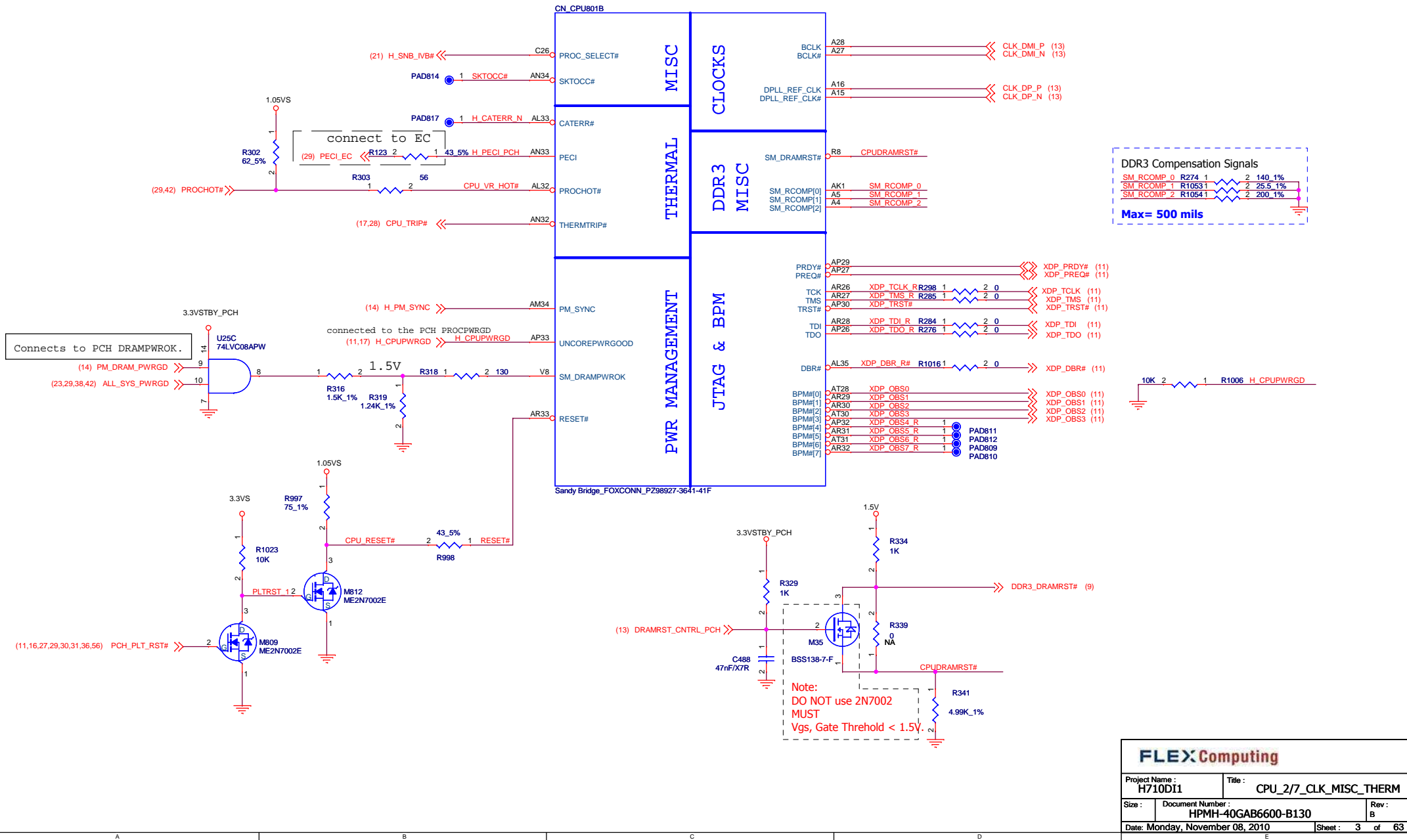
BACO 56

DGPU_PWROK 56
DGPU_PERST#

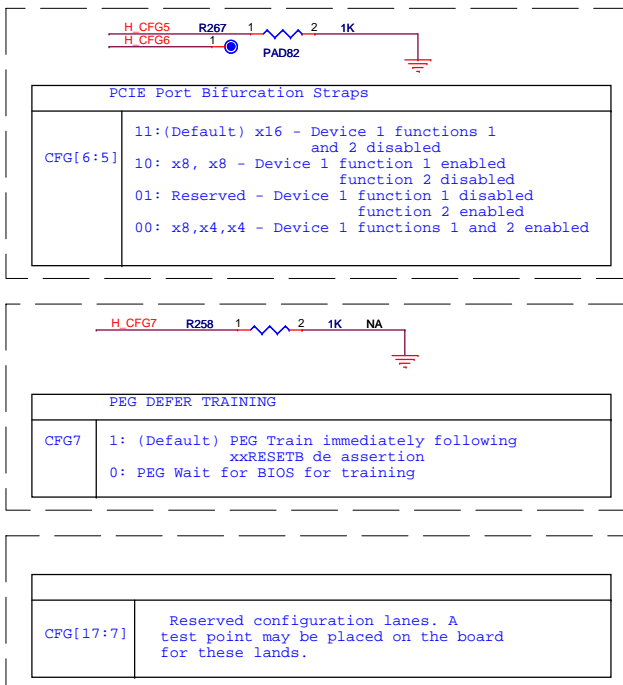
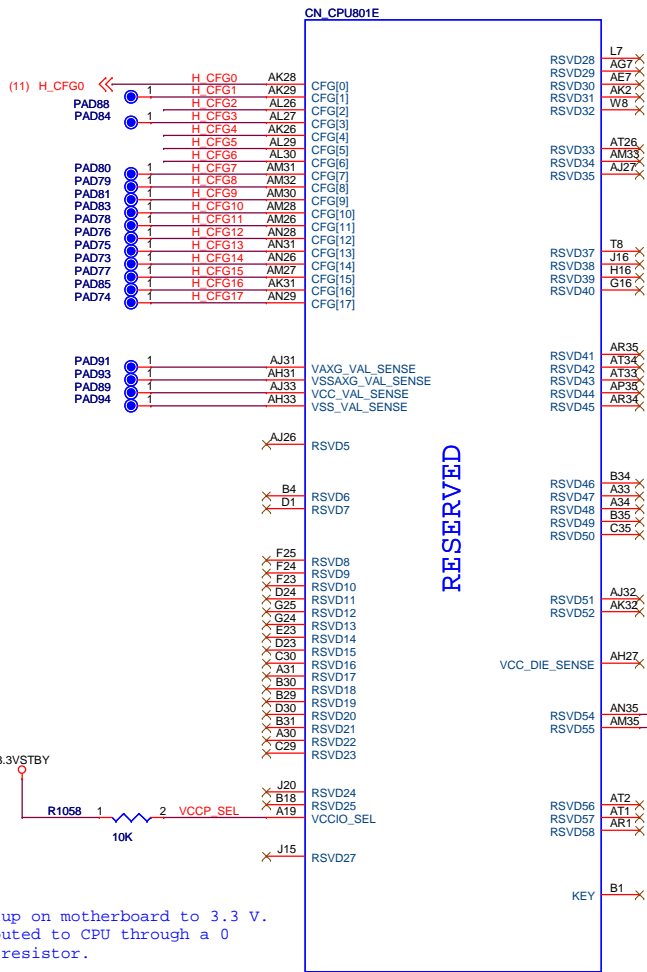


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Project Name: H710D11
Size: Document Number: HPMH-40GAB6
Date: Monday, November 08, 2010

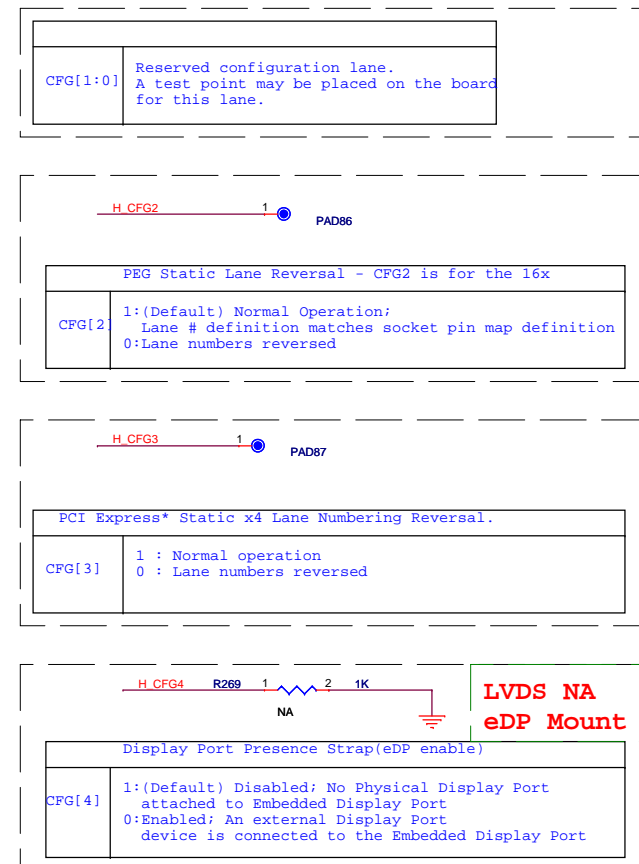
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Project Name : H710DI1		Title : CPU_2/7_CLK_MISC_THERM	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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CFG Straps for PROCESSOR



Pulled up on motherboard to 3.3 V.
Also routed to CPU through a 0 series resistor.

VCCIO_SEL On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Voltage selection for VCCIO: For Huron
River platforms, this pin must be pulled high
on the motherboard

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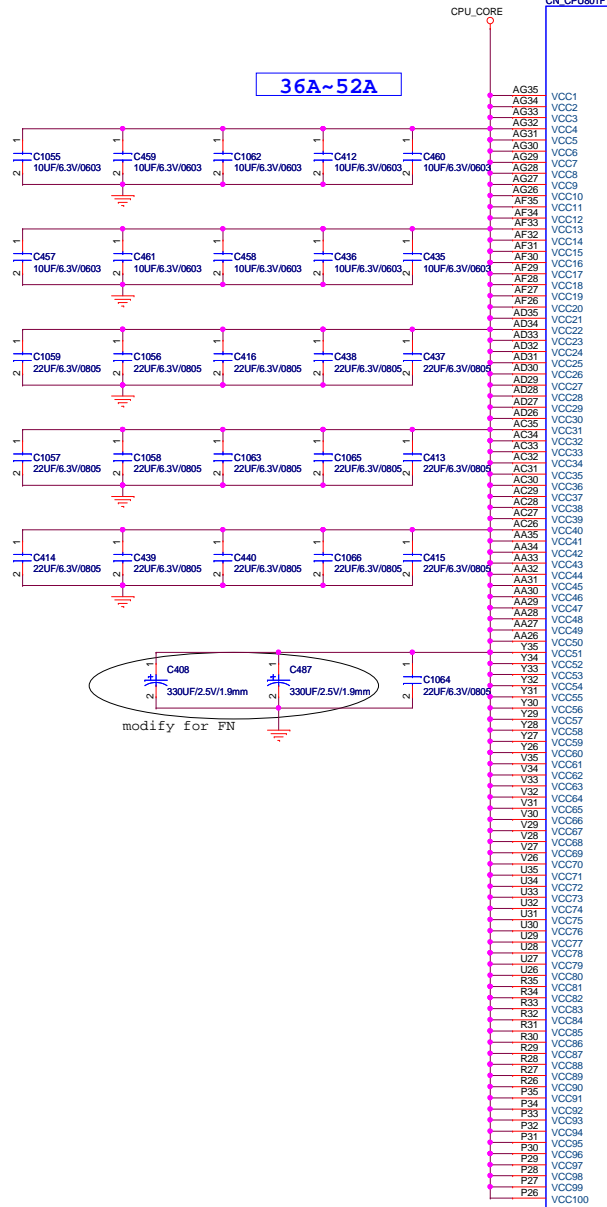
Project Name : H710DI1 Title : CPU_4/7_RSVD_CFG

Size : Document Number : HPMH-40GAB6600-B130

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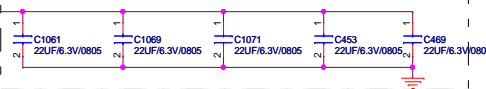
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POWER

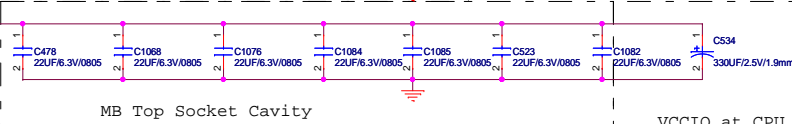


8.5A

MB Bottom Socket Cavity



MB Top Socket Cavity



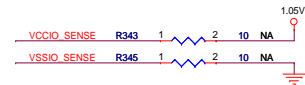
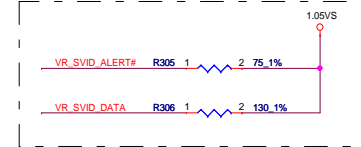
VCCIO at CPU

7/06 delet 330uF X2
poewr side have 330uF X3
(3x 330 μ F for 2012 capable designs)
follow Huron River Platform Power Delivery (439028)

50 ohm reference GND



Layout Note:
Alert#(AJ29) signal must be routed between
the Clock and Data lines to reduce the cross
talk between them. Spacing recommendations
from the "Asynchronous Signal General
Routing Guideline" of the Huron River
PDG have to be met.



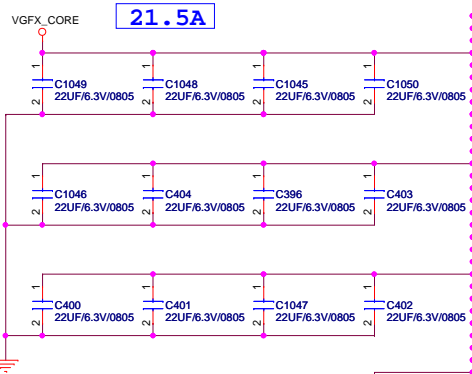
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Project Name:	H710D11	Title:	CPU_5/7_VCC_VCCIO
Size:	Document Number:	HPMH-40GAB6600-B130	Rev:
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POWER

CN_CPU801G



AT24 VAXG1
AT23 VAXG2
AT21 VAXG3
AT20 VAXG4
AT18 VAXG5
AT17 VAXG6
AR24 VAXG7
AR23 VAXG8
AR21 VAXG9
AR20 VAXG10
AR18 VAXG11
AR17 VAXG12
AP24 VAXG13
AP23 VAXG14
AP21 VAXG15
AP20 VAXG16
AP18 VAXG17
AP17 VAXG18
AN24 VAXG19
AN23 VAXG20
AN21 VAXG21
AN20 VAXG22
AN18 VAXG23
AN17 VAXG24
AM24 VAXG25
AM23 VAXG26
AM22 VAXG27
AM20 VAXG28
AM18 VAXG29
AM17 VAXG30
AL24 VAXG31
AL23 VAXG32
AL21 VAXG33
AL20 VAXG34
AL18 VAXG35
AL17 VAXG36
AK24 VAXG37
AK23 VAXG38
AK21 VAXG39
AK20 VAXG40
AK18 VAXG41
AK17 VAXG42
AJ24 VAXG43
AJ23 VAXG44
AJ20 VAXG45
AJ18 VAXG46
AJ17 VAXG47
AJ16 VAXG48
AH24 VAXG49
AH23 VAXG50
AH21 VAXG51
AH20 VAXG52
AH18 VAXG53
AH17 VAXG54

SENSE
LINES

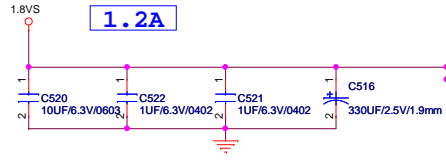
VREF

DDR3 - 1.5V RAILS

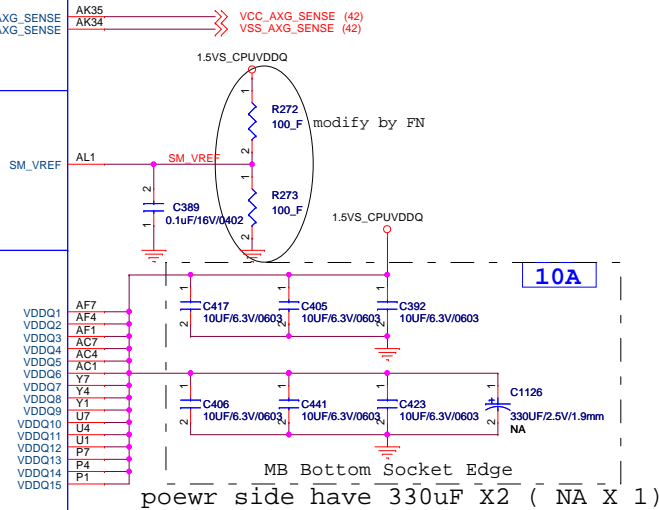
SA RAIL

MISC

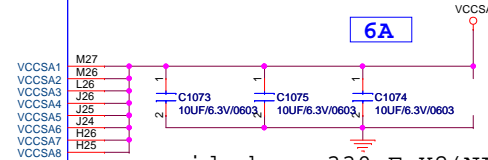
1.8V RAIL



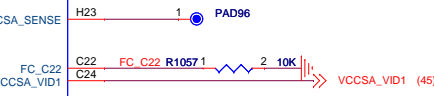
Sandy Bridge_FOXCONN_P298927-3641-41F



poewr side have 330uF X2 (NA X 1)

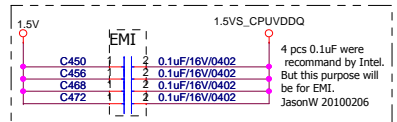


poewr side have 330uF X2(NA)

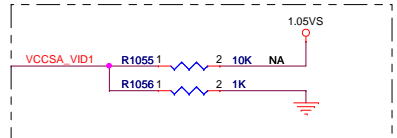


VCCSA_SEL Voltage Selection Table

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	2011 processor	2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes



Layout
Four 0402 0.1uF stitching capacitors added between +V1.5_DIMM & +V1.5S_CPU_VDDQ S3PowerReduction checklist

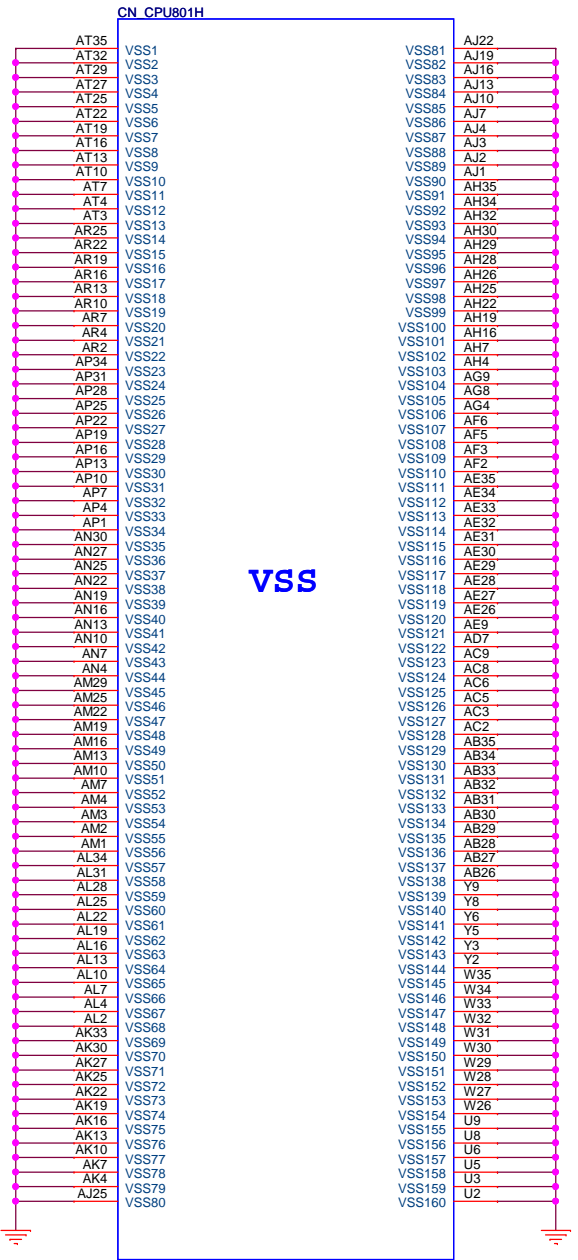
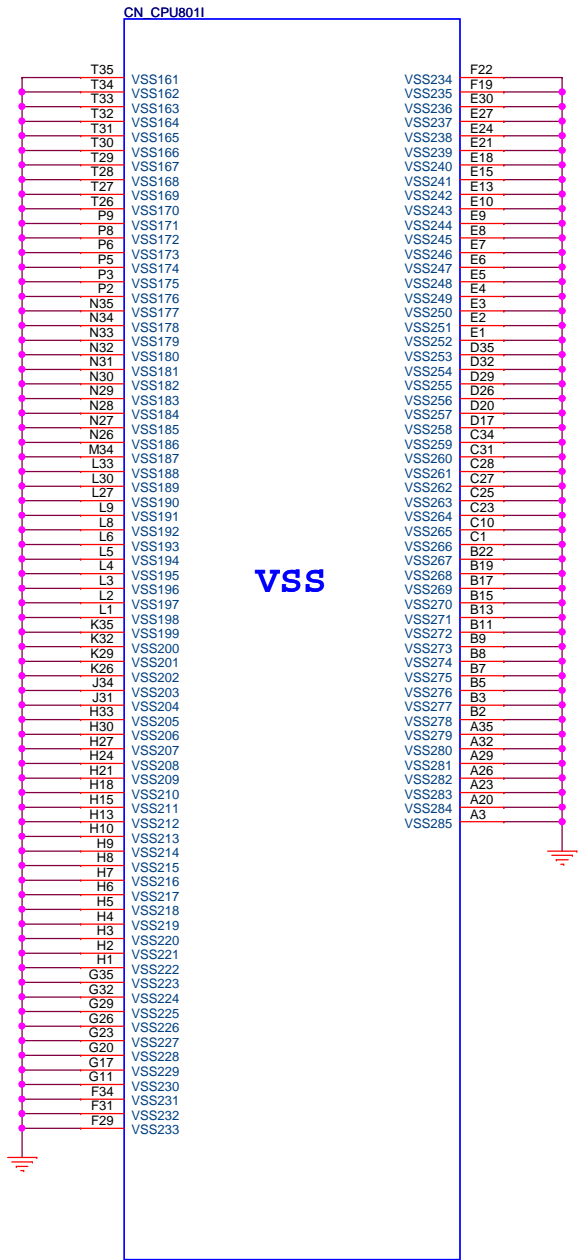


1. MB Bottom Socket Cavity 10uFX2
2. MB Bottom Socket Edge 10uFX1
3. VCCSA at processor

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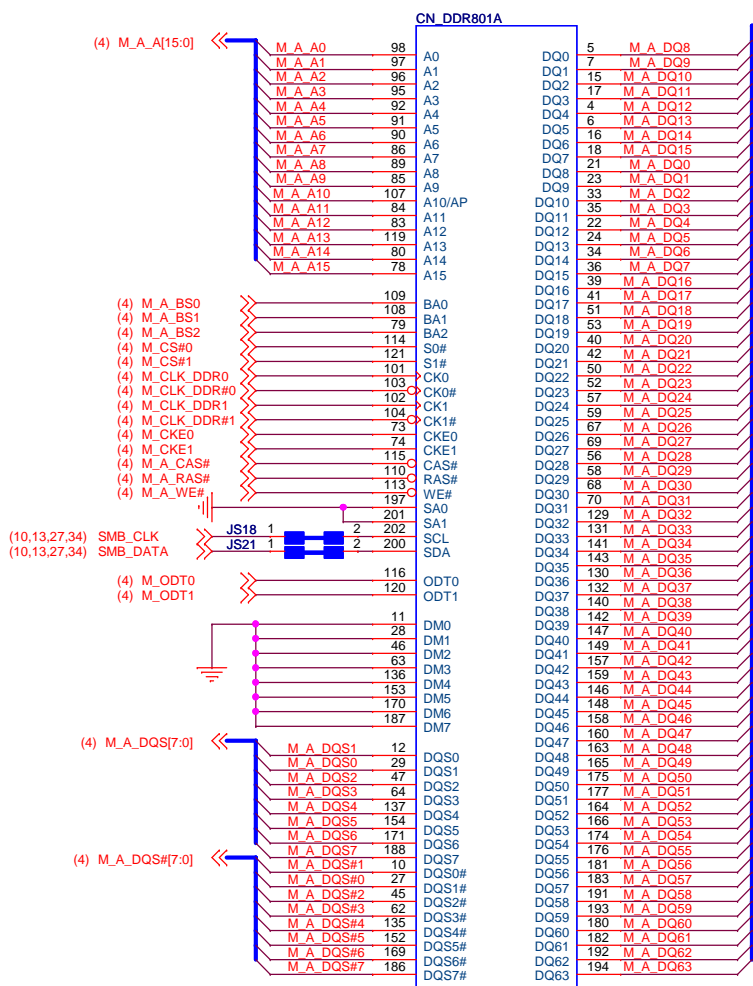
Project Name : H710DI1	Title : CPU_6/7_VGFX_VDDR3
Size : HPMH-40GAB6600-B130	Rev : B
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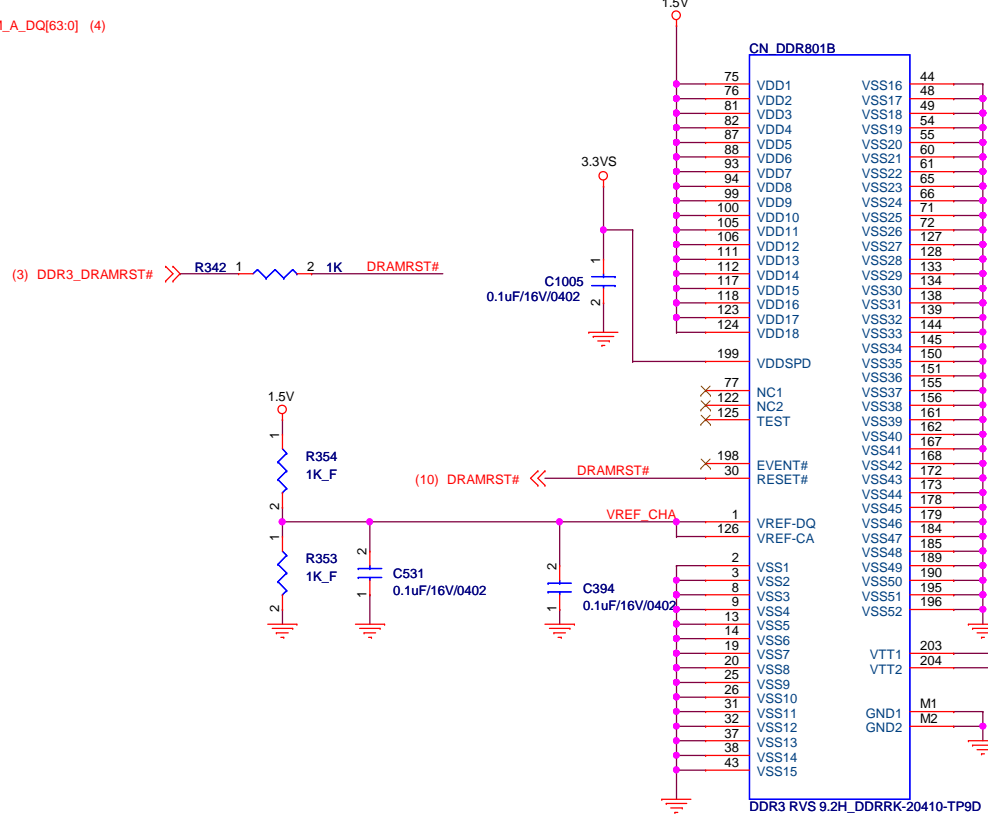
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Project Name : H710DI1		Title : CPU_7/7_VSS	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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Channel-A

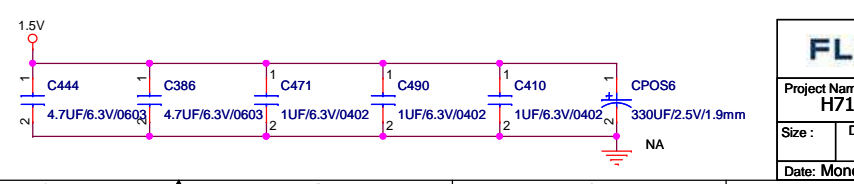
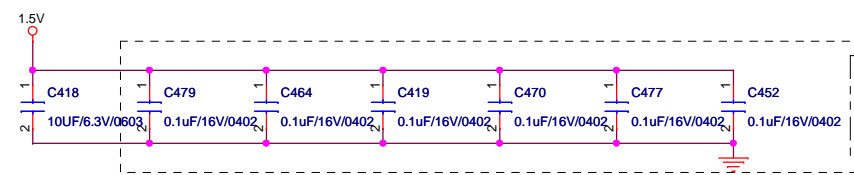


DDR3 RVS 9.2H_DDRRK-20410-TP9D
CONN DDR3 RVS DDRRK-20410-TP9D 204P 9.2H

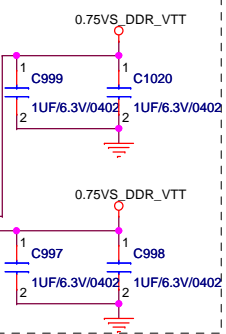
Note:
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30



CONN DDR3 RVS DDRRK-20410-TP9D 204P 9.2H



Layout
Place these caps close to Pin203 and 204.

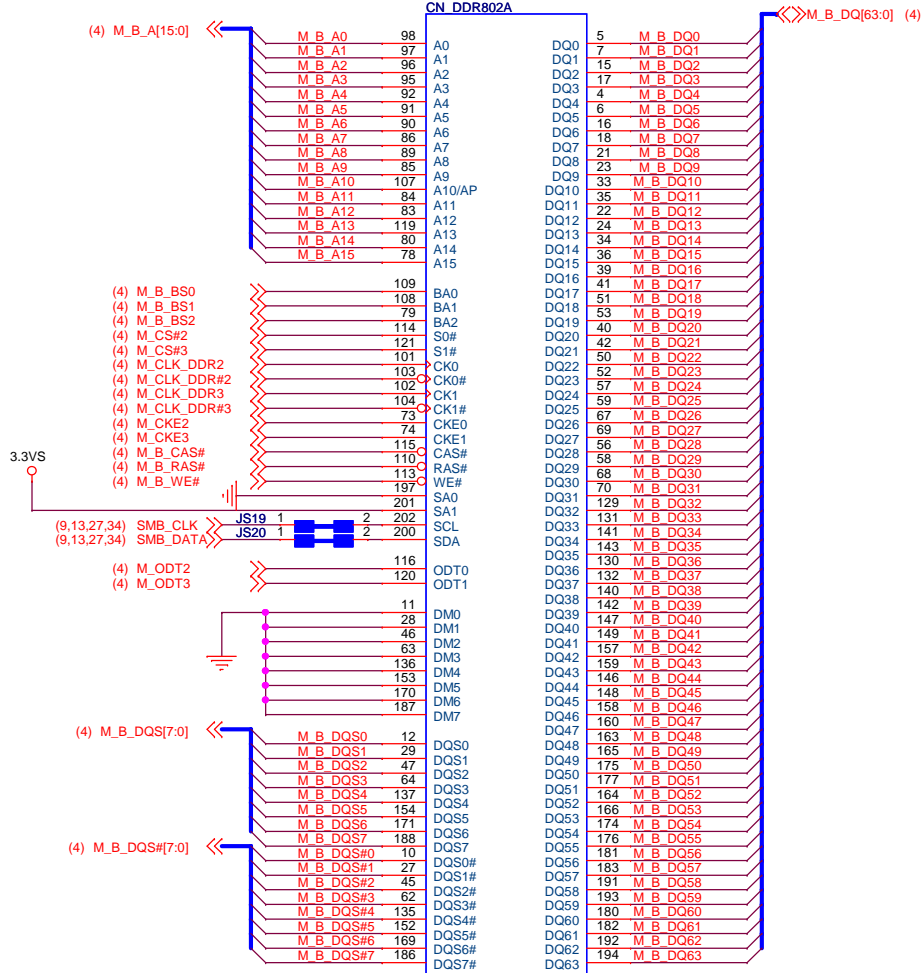


Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206

Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin.

FLEXComputing			
Project Name :		Title :	
H710DI1		DDR3_SO-DIMM1_CHA(9H2)	
Size :	Document Number :	Rev :	
	HPMH-40GAB6600-B130	B	
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Channel-B

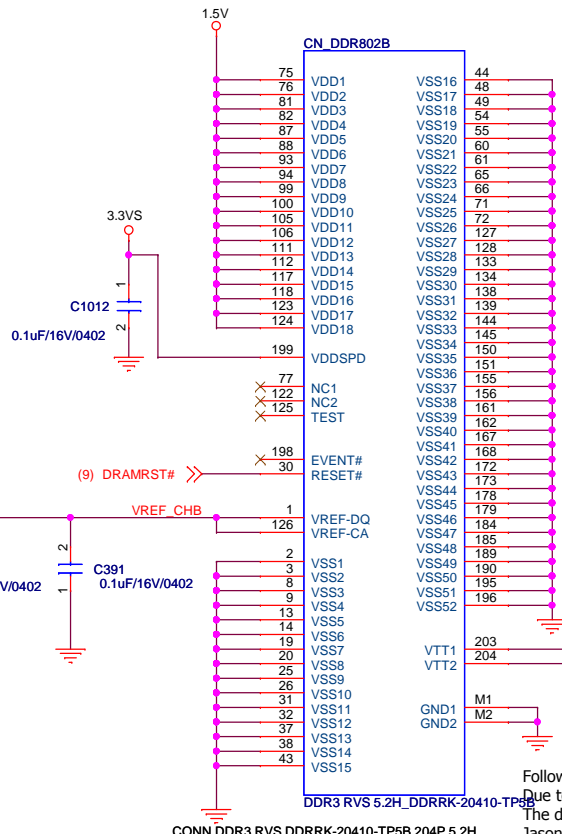


DDR3 RVS 5.2H_DDRRK-20410-TP5B
CONN DDR3 RVS DDRRK-20410-TP5B 204P 5.2H

SO-DIMM Address			
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0	
	TS	0x30	
SA0_DIM1 = 0, SA1_DIM1 = 1	SPD	0xA4	
	TS	0x34	

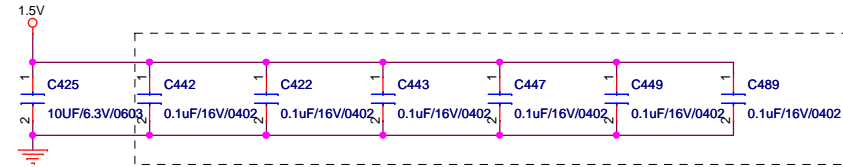
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

7/26 Matutina Modify



Layout
Place these caps close to Pin203 and 204.

Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206

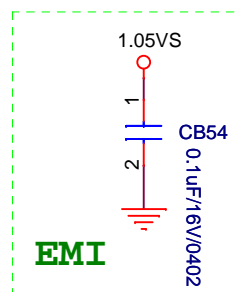
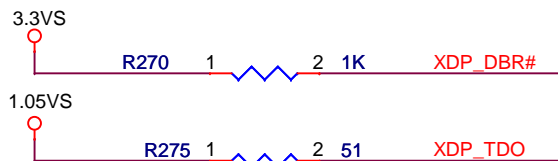
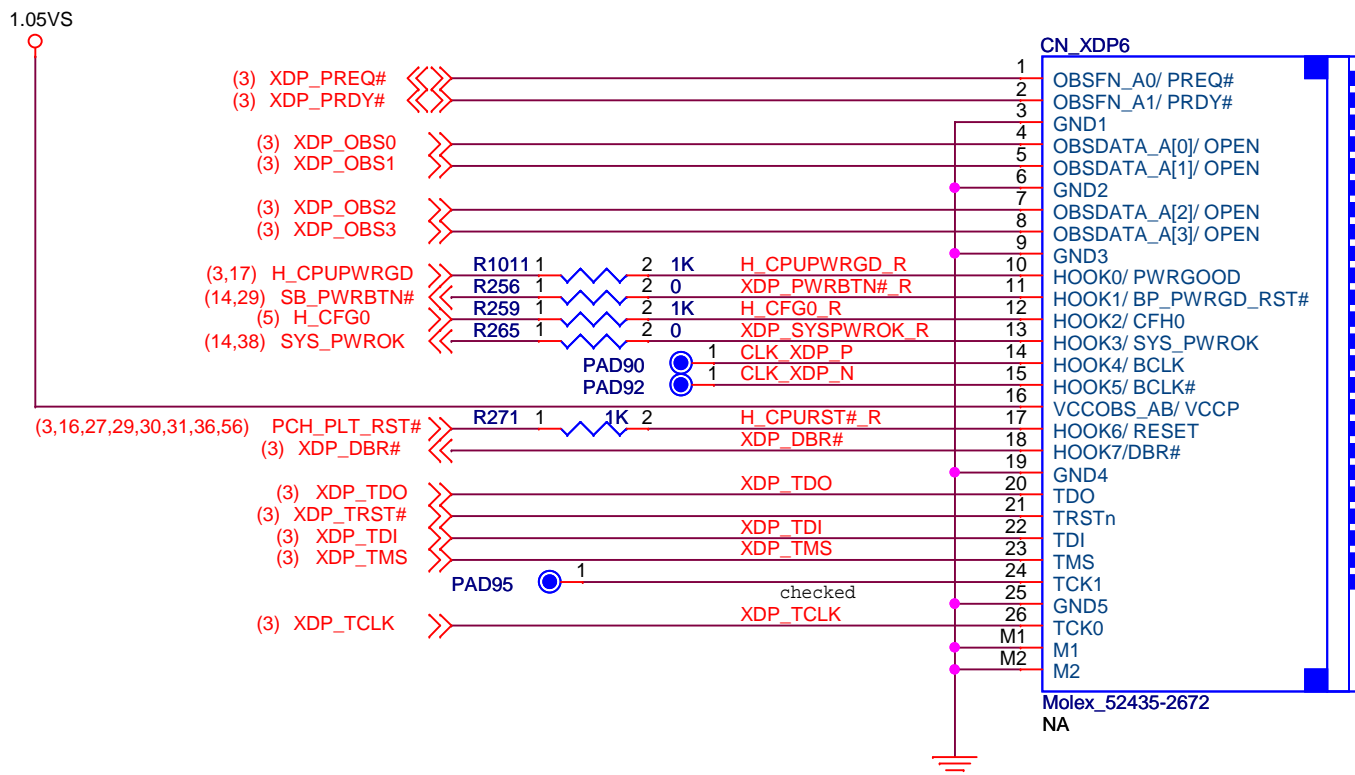


Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin .

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Project Name : H710DI1	Title : DDR3_SO-DIMM2 CHB(5H2)
Size : HPMH-40GAB6600-B130	Rev : B
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Debug Port



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Project Name :
H710DI1

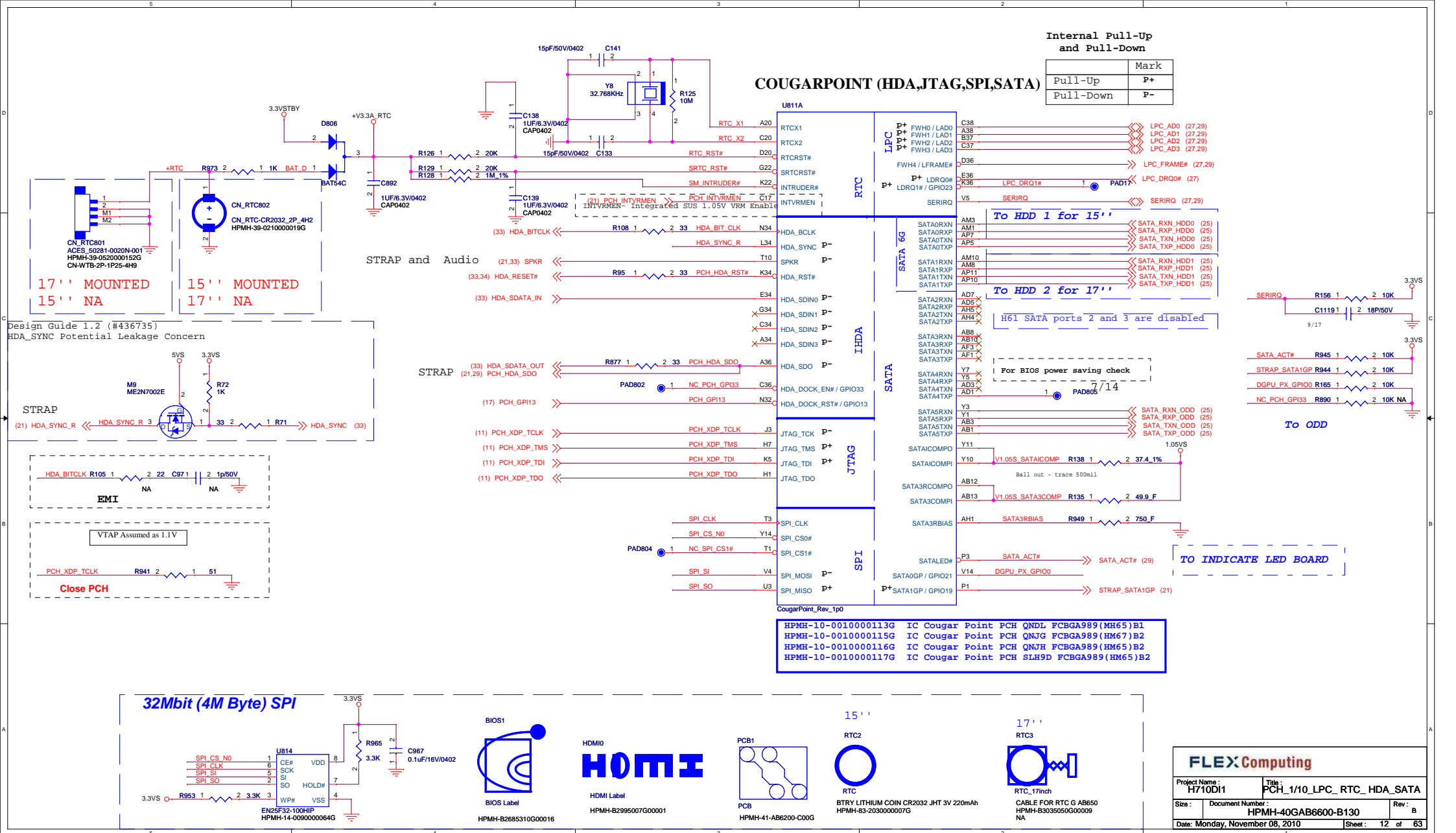
Title :
XDP(PROCESSOR / PCH)

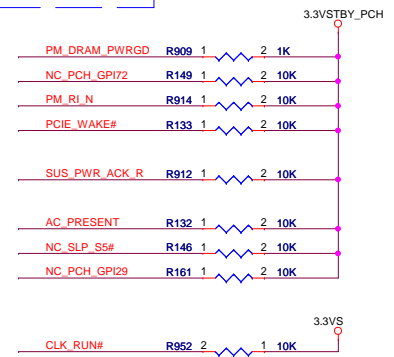
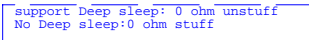
Size :

Document Number :
HPMH-40GAB6600-B130

Date: Monday, November 08, 2010

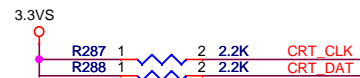
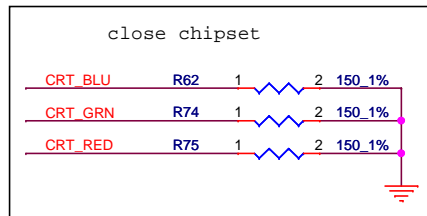
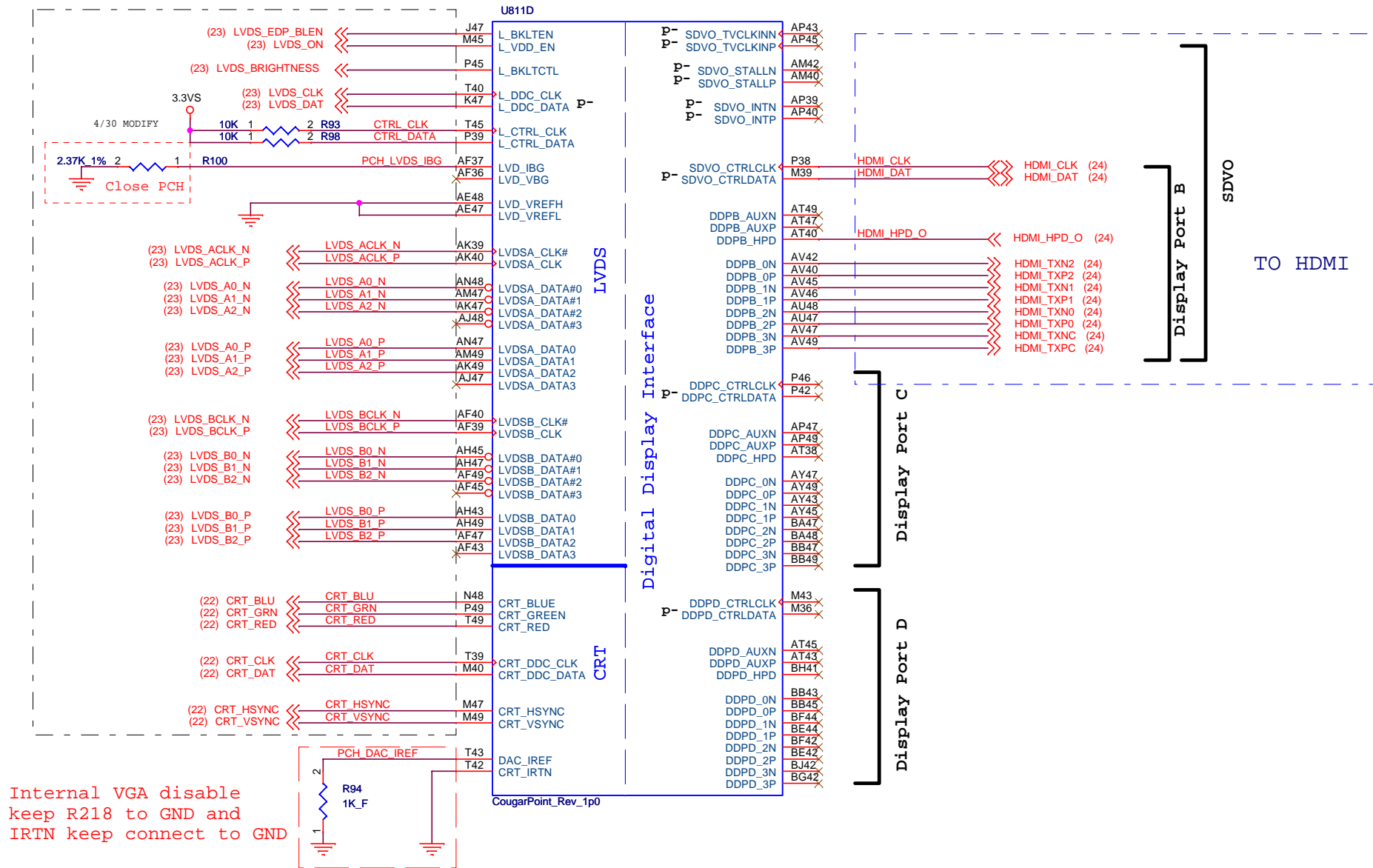
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The BATLOW# input can inhibit waking from S3, S4, and S5 states if there is no sufficient power if use connect from EC

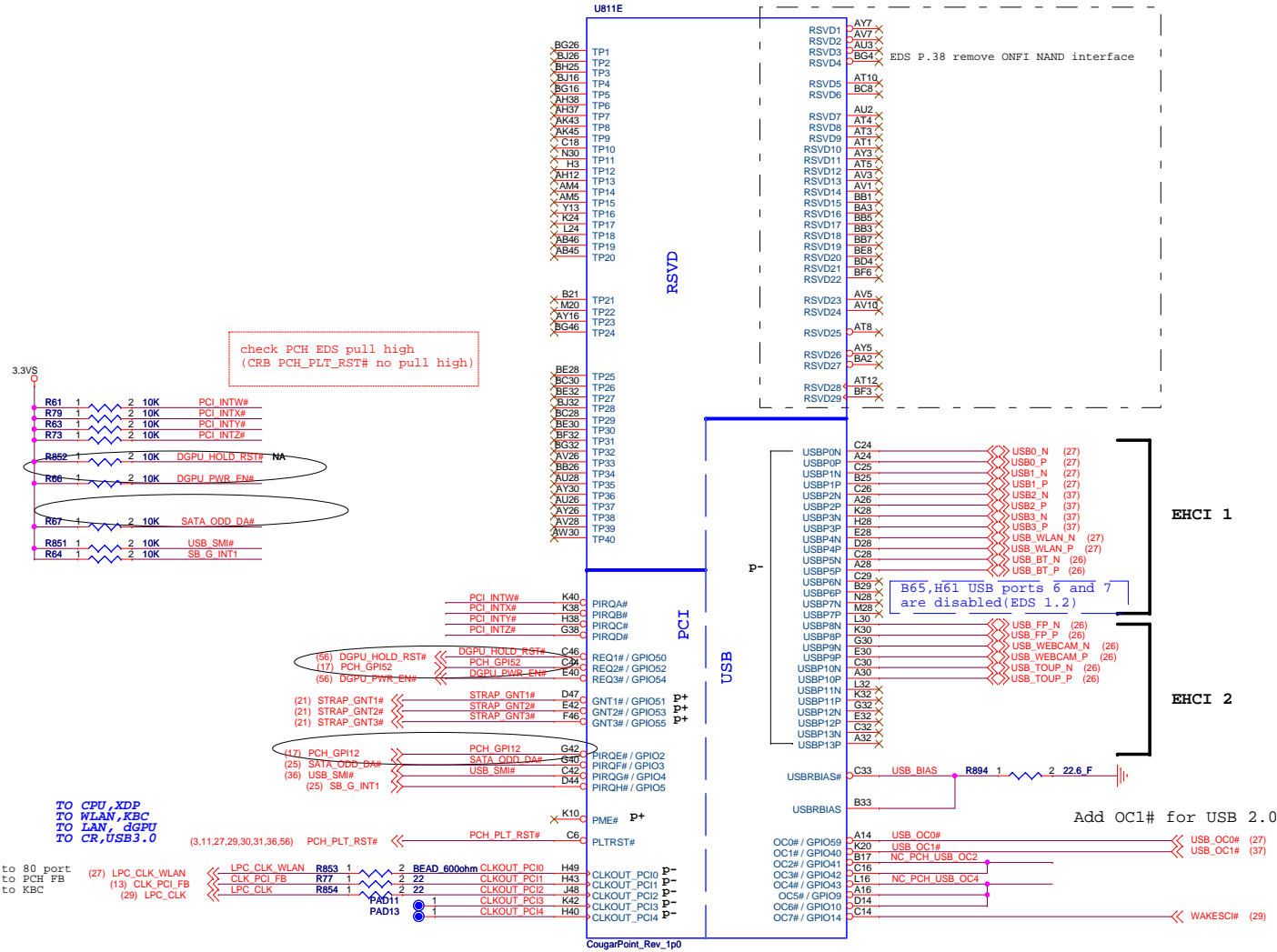
COUGARPOINT (LVDS,DDI)



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Project Name : H710D11	Title : PCH
Size : Document Number : HPMH-40GAB	
Date: Monday, November 08, 2010	

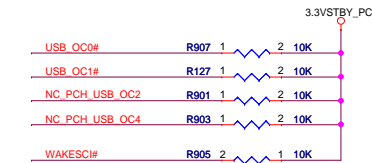
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COUGARPOINT (PCI,USB,NVRAM)

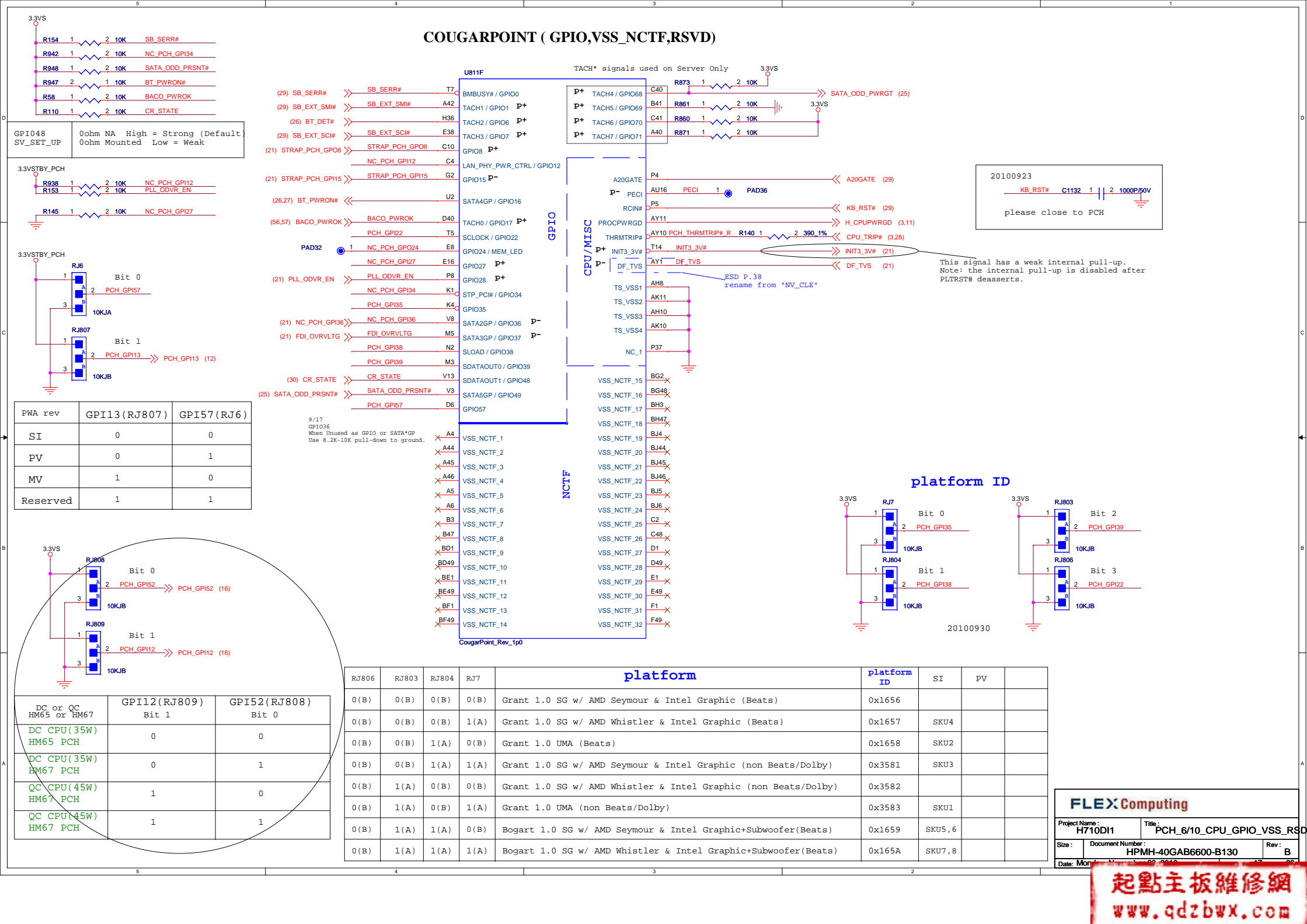


DB-USB Port 0	OC0
DB-USB Port 1	OC1
MB-USB Port 2	
MB-USB Port 3	
USB-WLAN Port 4	
USB-BT Port 5	
USB-FT Port 8	
USB-WEBCAM Port 9	
USB-TOUCH SCREEN PORT 10	
*USB-Port1 and port9 for BIOS debug tool	

1. 14 USB ports are not available on all Standard SKU's.
2. SFF USB ports are only 12 port



COUGARPOINT (GPIO,VSS_NCTF,RSVD)



U811G	POWER

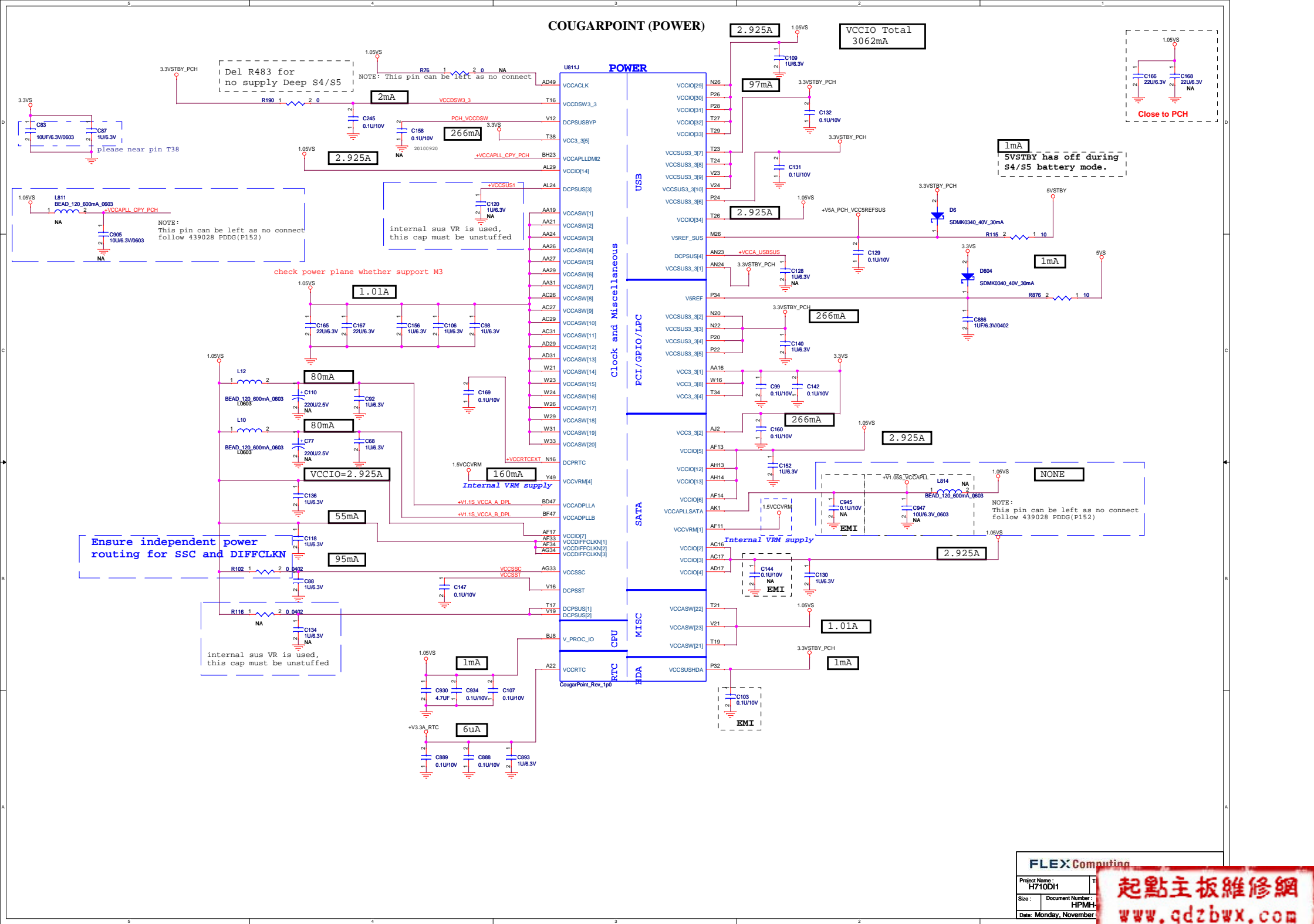


Title : PCH_7/10_POWER 1

Rev : B

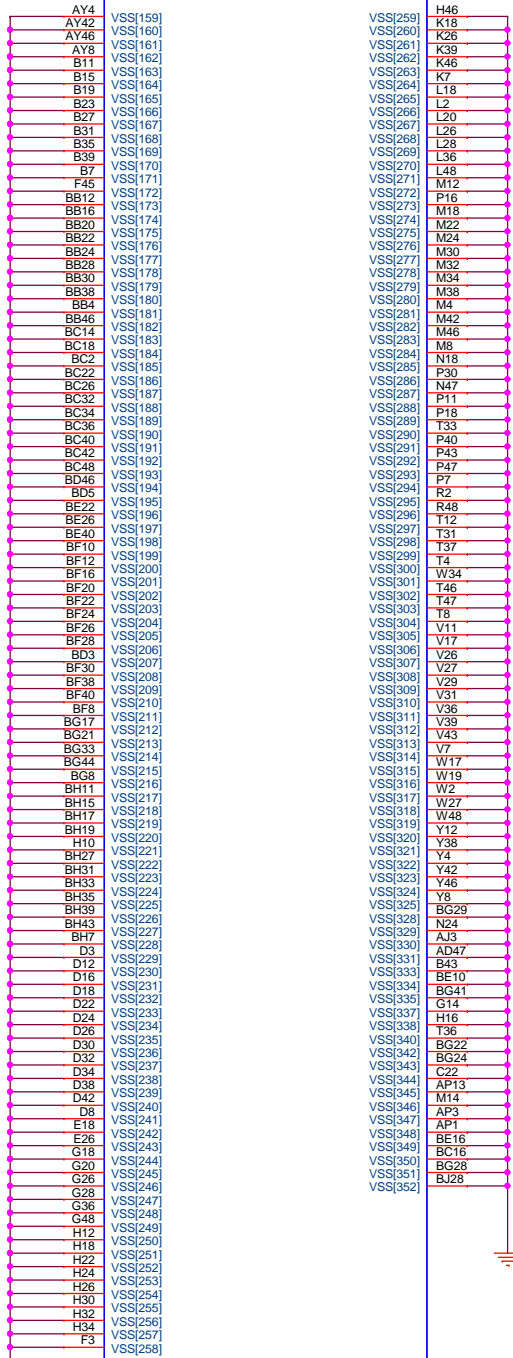
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COUGARPOINT (POWER)



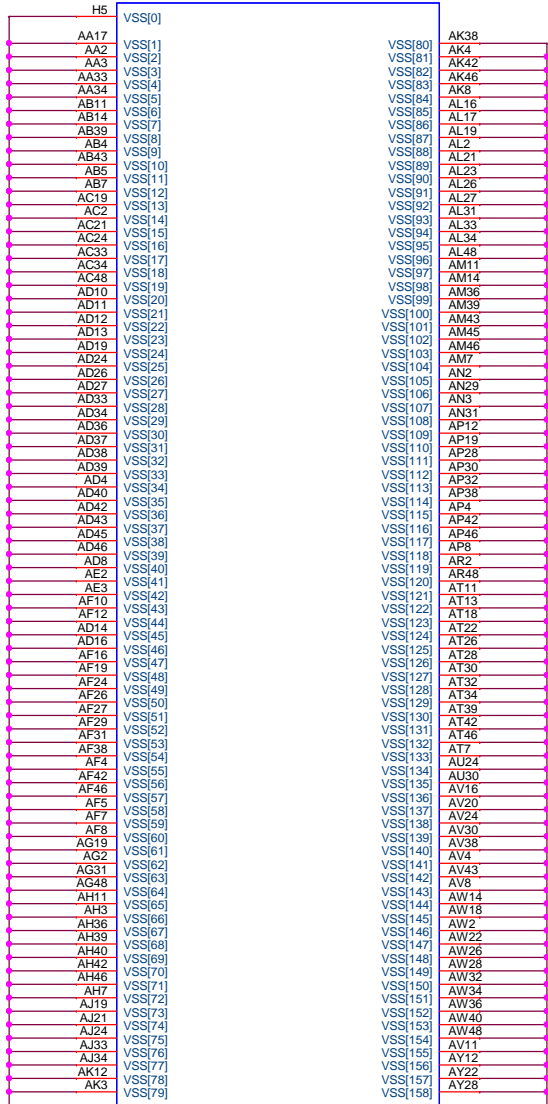
COUGARPOINT (GND)

U811I



CougarPoint_Rev_1p0

U811H



CougarPoint_Rev_1p0

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Project Name :
H710D11

Title :
PCH_9/

Size : Document Number :
HPMH-40GAB6600-B13

Date: Monday, November 08, 2010

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Signal	Usage	When Sampled	Internal PULL	Comment
SPKR	No Reboot	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: If the signal is sampled high, this indicates that the system is strapped to the No Reboot mode L: Cougar Point will disable the TCO Timer system reboot feature (Chipset Config Registers' Offset (3410h:Bit 5)). Default
INIT3_3V#	Reserved	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	This signal should not be pulled low
GNT[3]#/GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Top Block Swap Mode disabled Default L: If the signal is sampled low, this indicates that the system is strapped to the Top Block swap mode
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	NA	H: Integrated 1.05V VRMs enabled Default This signal should always be External pulled high L: Integrated 1.05V VRMs disabled
GNT1#/GPIO51/ BBS[1]	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	GNT1# SATA1GP Boot BIOS Location 0 0 LPC 0 1 Reserved 1 0 PCI 1 1 SPI Default
SATA1GP/ GPIO19	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	
GNT2#/GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Should not be pulled low for desktop and mobile ESI compatible mode is for server platforms only. Default L: Configures DMI for ESI compatible operation
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Internal PD	H: If sampled high,the Flash Descriptor Security will be overridden. L: If strap is sampled low, (Default) the security measures defined in the Flash Descriptor will be in effect. This signal should not be pulled high
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	Internal PD	The internal pull-down is disabled after PLTRST# deasserts
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Internal PU	H: The On-Die PLL voltage regulator is enabled when sampled high Default L: When sampled low the On-Die PLL Voltage Regulator is disabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	Internal PD	H: On-Die PLL VR is supplied by 1.5 V Default L: On-Die PLL VR is supplied by 1.8 V
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Internal PD The weak internal pull-down is disabled after RSMRST# deasserts	H: Intel ME Crypto TLS cipher suite with confidentiality Default L: Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	Internal PD The internal pull-down is disabled after PLTRST# deasserts.	H:LVDS is detected Default L:LVDS is not detected
SDVO_CTLRLDATA	Port B Detected	Rising Edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H:Port B is detected L:Port B is not detected Default
DDPC_CTLRLDATA	Port C Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port C is detected L: Port C is not detected Default
DDPD_CTLRLDATA	Port D Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port D is detected L: Port D is not detected Default
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	NA	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: NOTE: This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST#	Internal PU (Pull-up is disabled after RSMRST# is deasserted.)	NOTE: This signal should not be pulled low

PAD24 1 SPKR (12,33)

PAD21 1 INIT3_3V# (17)

R70 1 2 1K NA STRAP_GNT3# (16)

+V3.3A_RTC
R896 1 2 330K PCH_INVRMEN (12)

R69 1K NA R943 1K NA
STRAP_GNT1# (16)
STRAP_SATA1GP (12)

PAD10 1 STRAP_GNT2# (16)

3.3VS
R1115 1 2 1K NA PCH_HDA_SDO (12,29)

1.8VS R933
PLACE 2.2K CLOSE TO THE BRANCHING POINT
(3) H_SNB_IVB# R929 1 2 1K DF_TVS (17)

PAD35 1 PLL_ODVR_EN (17)

3.3VSBY_PCH
R107 1 2 1K HDA_SYNC_R (12)

3.3VSBY_PCH
R939 1 2 1K NA STRAP_PCH_GPI15 (17)

+V3.3A_RTC
R1067 1 2 330K
R899 1 2 330K NA DSWODVRN (14)

R1110 1 2 10K NC_PCH_GPI36 (17)

R151 1 2 10K FDI_OVRVLGT (17)

R918 1 2 1K STRAP_PCH_GPO8 (17)

NO REBOOT	
NA	Low=Disable(Default)
MOUNTED	High=Enable

A16 swap override Strap	
STP_A160VR	Low = A16 swap override High = Default

INTVRMEN- Integrated SUS
1.05V VRM Enable

Flash Descriptor Security Override	
PCH_HDA_SDO	NA Low=Disable(Default) MOUNTED High=Enable

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

PLL ON DIE VR ENABLE	
PLL_ODVR_EN	ENABLE- UNSTUFF DISABLE-STUFF

HR only support 1.5 V
HDA_SYNC need PU to HDA SUS rail through 1k ohm
for 451710_451710 SPEC

DSWODVRN - On Die DSW VR Enable	
Pull High	Enable (Default)
Pull Down	Disable

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

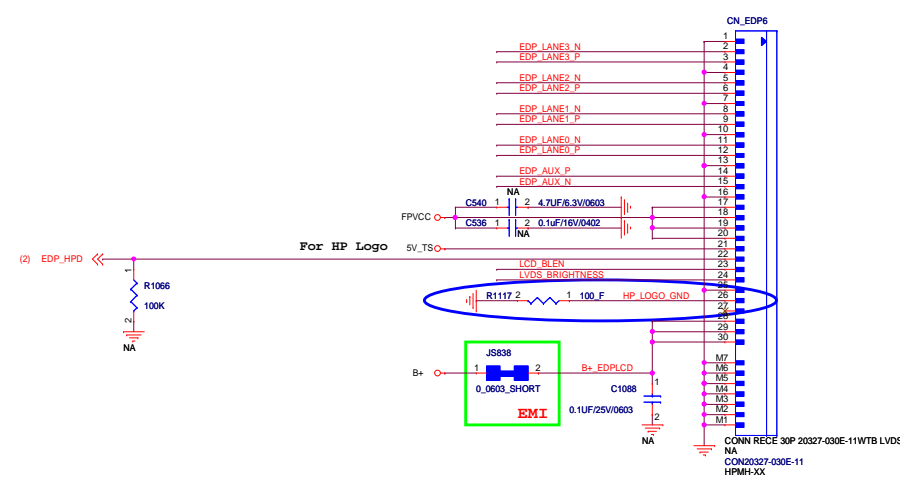
FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLGT)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

GPIO8 Integrated Clock Chip Enable	
High	Disable
Low	Enable(default)

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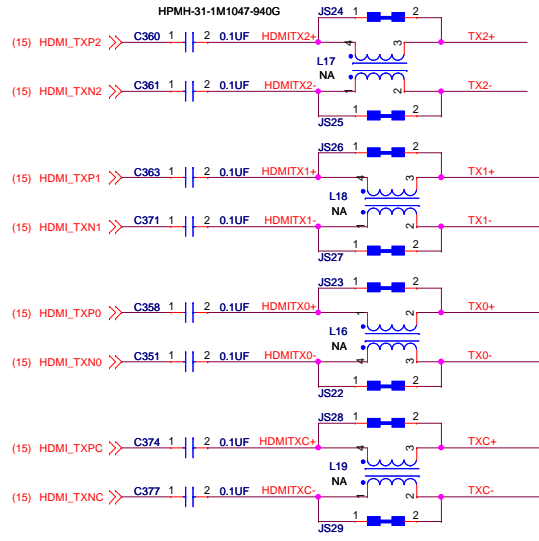
Project Name : H710DI1	
Size : Document Number : HPM	
Date : Monday, November	

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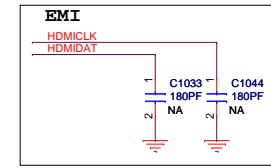
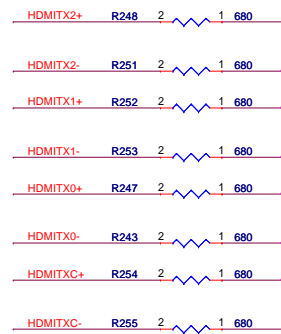


HDMI

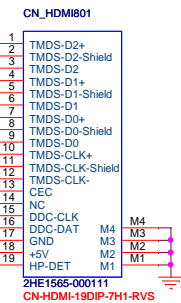
CLOSE to CN_HDMI1
HPMH-32-4000000104G



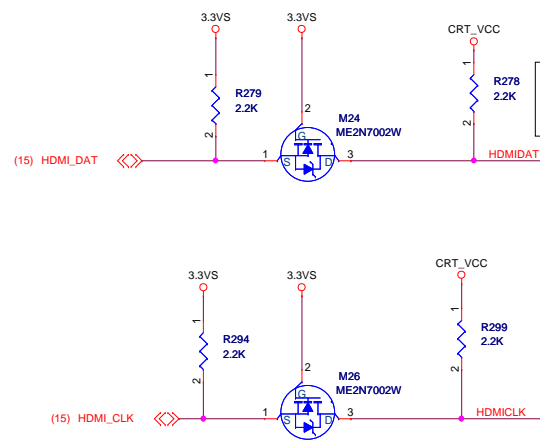
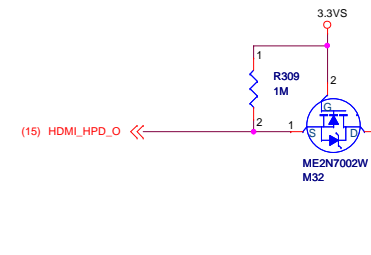
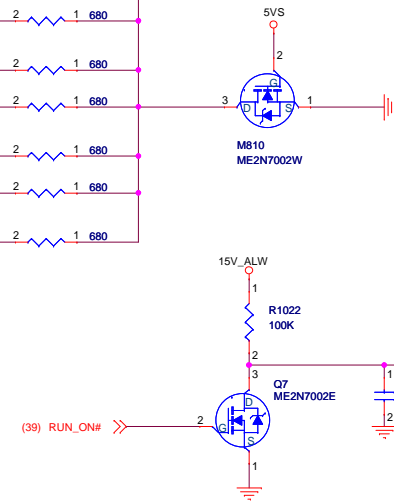
Intel Huron River: 680 ohm
AMD Danube: 715 ohm
AMD Sabine: 715 ohm



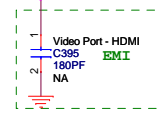
HDMI



2HE1565-00011
CN-HDMI-19DIP-7H1-RVS
HPMH-38-00F0000017G



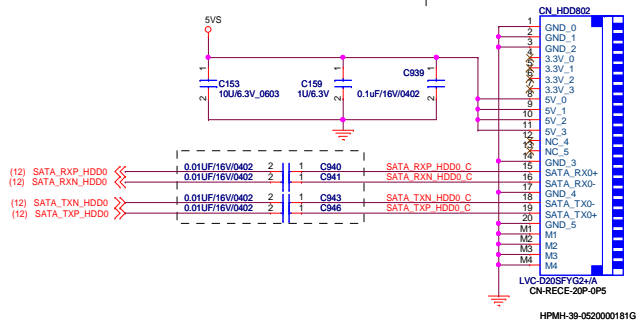
HDMI test
C1 -- Cp=45pf
C2 -- Cp=46pf (spec<50pf)



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Project Name : H710DI1		Title : HDMI CONN	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date : Monday, November 08, 2010		Sheet : 24 of 63	

HDD

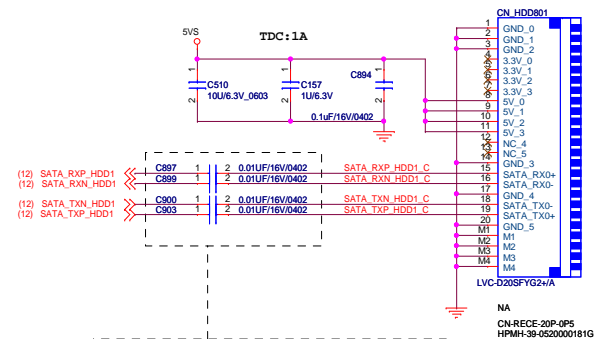
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist



2nd HDD

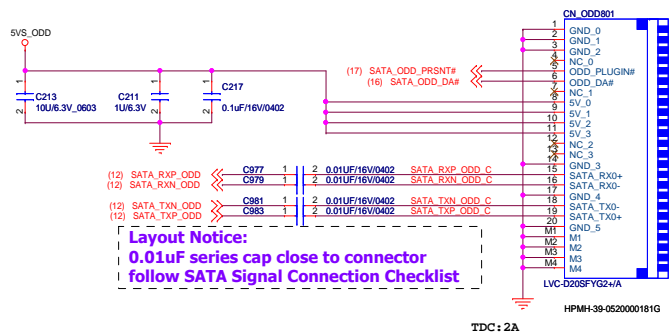
FOR 17" MB USE WTB CONNECTOR

CONN SPEC: 0.3A/PIN



Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

ODD



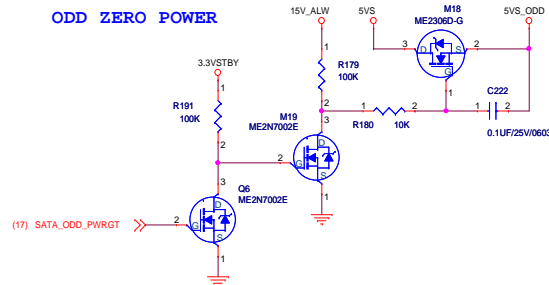
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

TDC: 2A

Change to Cable type Conn

ODD Zero Power

Check if meet max current!!



G-Sensor

G-SENSOR

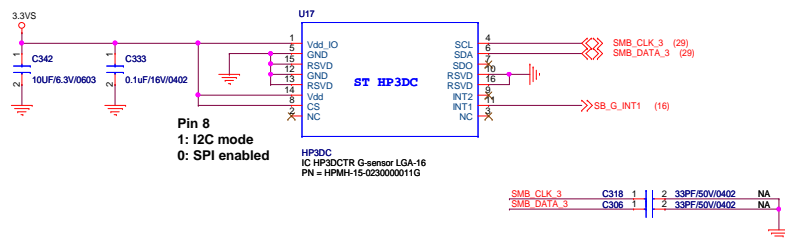
ST HP3DC

3.3VS

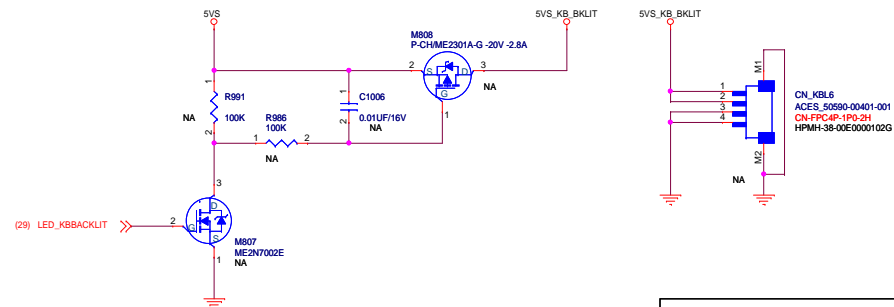
ADDR: 0011000x(30h) - SDO PD

ADDR: 0011010x(32h) - SDO NC

SINK: ??mA@VoL=0.33V(MAX)



KB Backlit

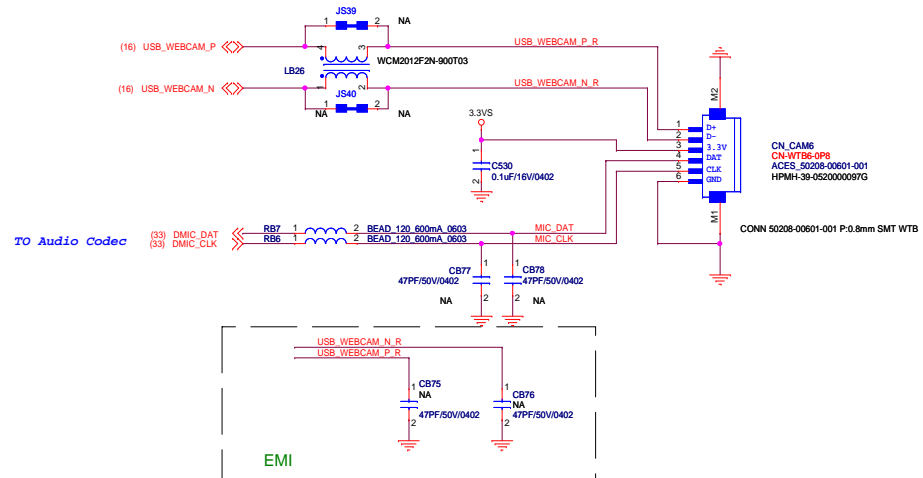


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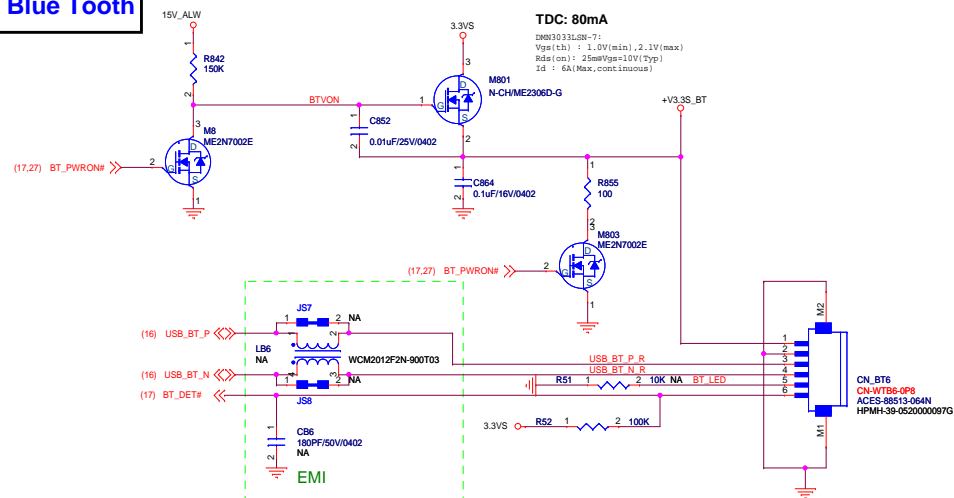
Project Name :
H710D11
Size :
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Date : Monday, November

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Web CAM



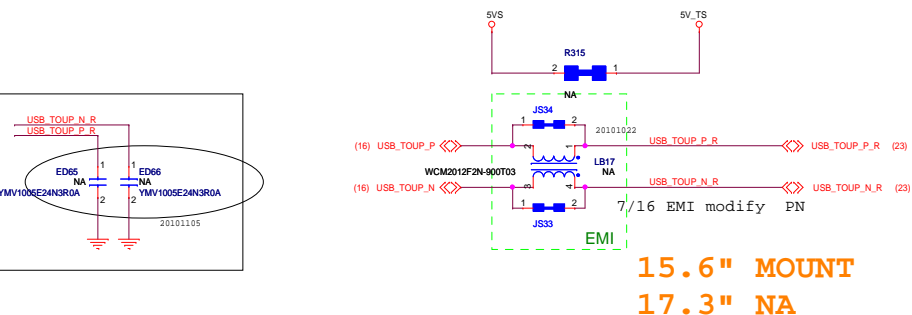
Blue Tooth



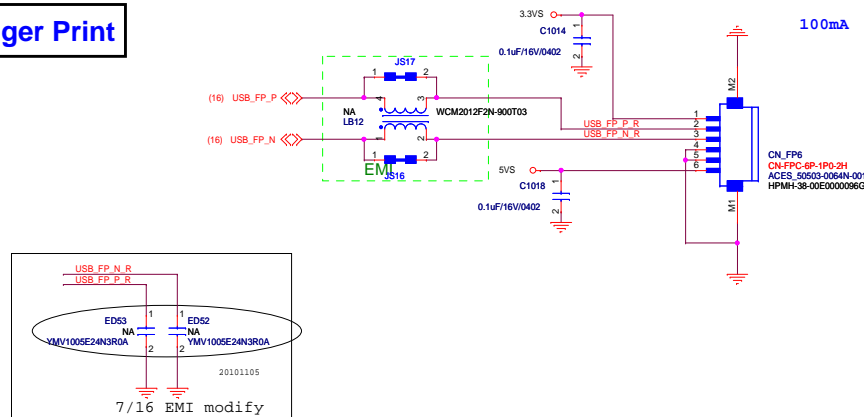
TouchScreen

Touch Screen power is 5V type

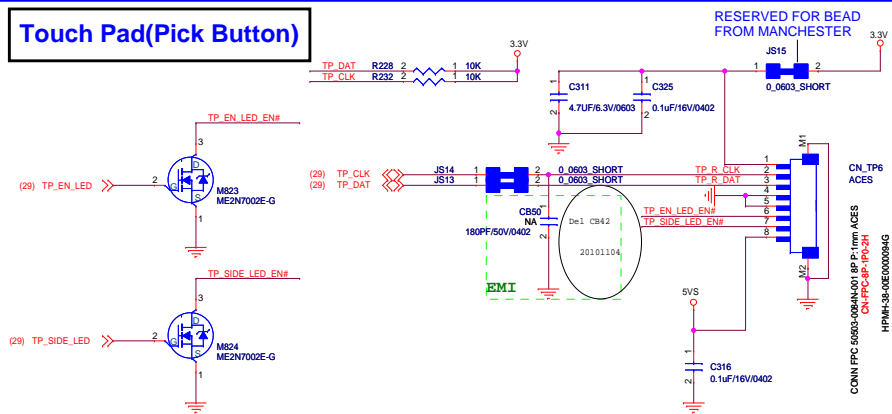
Peak 200mW 40mA



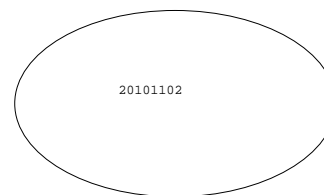
Finger Print



Touch Pad(Pick Button)



LID

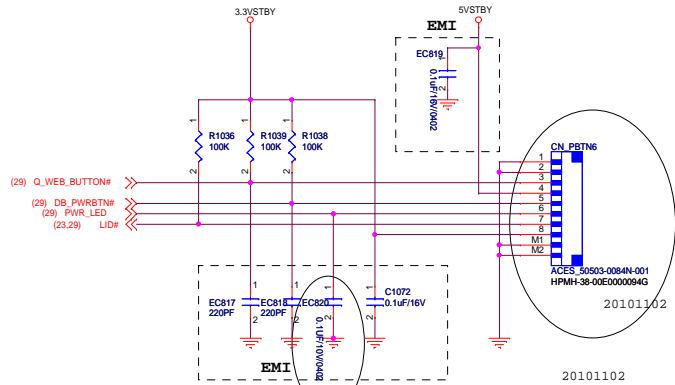


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Project Name :		H710DI1
Size :	Document Number :	
	HPMH-	
Date: Monday, November		

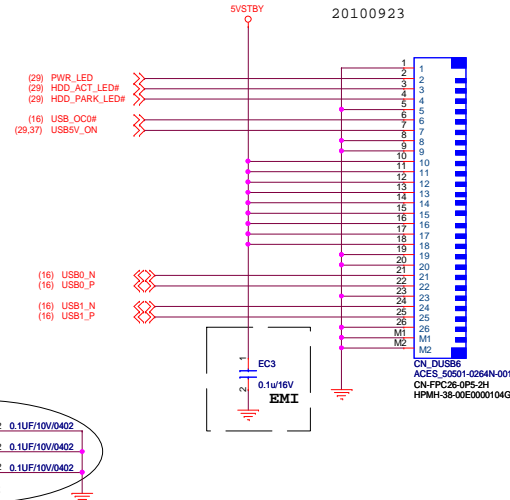
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PWRBTN BOARD

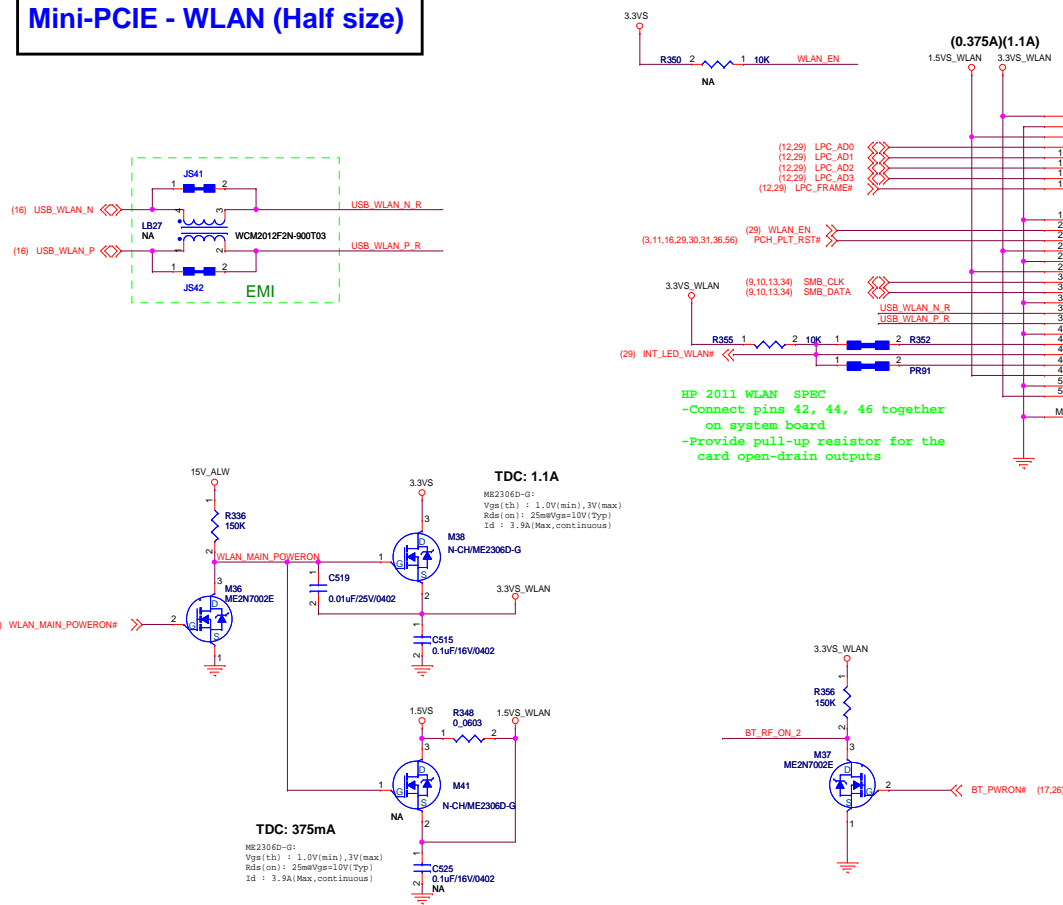


connector on Mother Board for
Power Button/LED/LID Daughter board

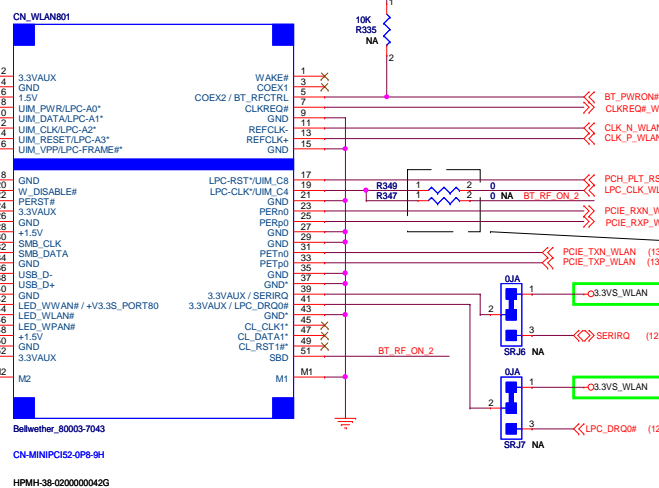
USB BOARD



Mini-PCIE - WLAN (Half size)



WLAN CONNECTOR



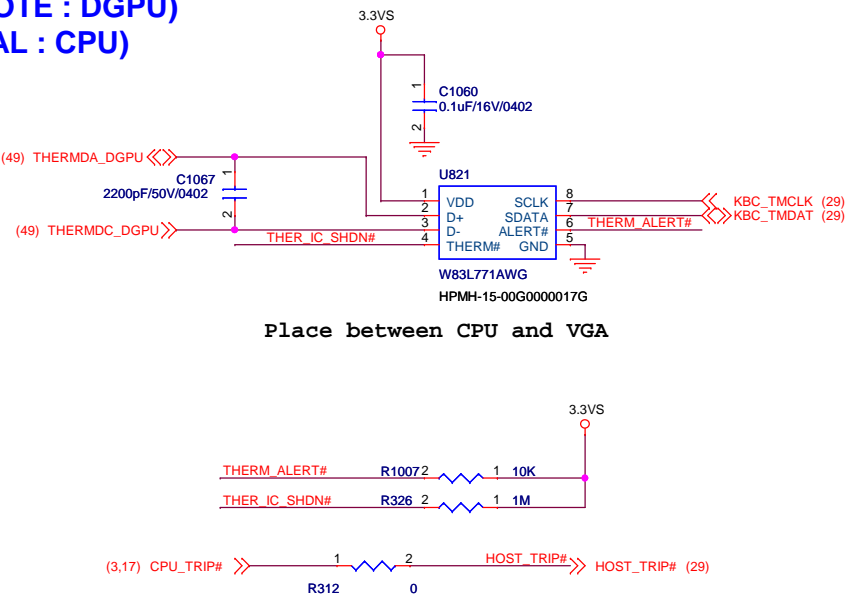
HP 2011 WLAN SPEC 2nd RF ON/OFF Pin
Primary path is to implement it on pin 51,
but 0 Ohm strap to pin 19 required for
Intel Rainbow Peak ES2 cards use
(QS will transition to pin 51).

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Project Name: H710D11
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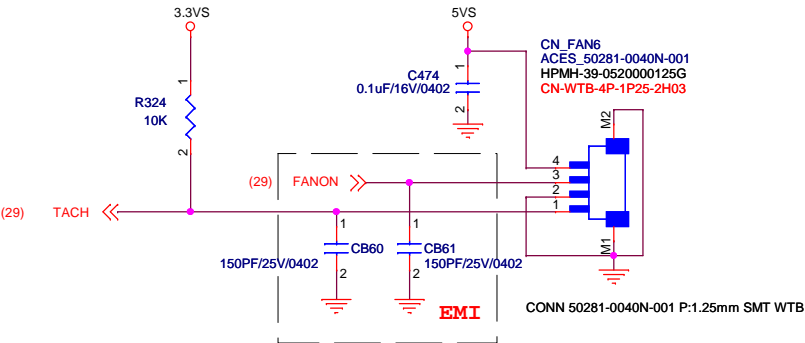
Thermal Sensor
(REMOTE : DGPU)
(LOCAL : CPU)



THERMAL IC FOR CPU or DGPU

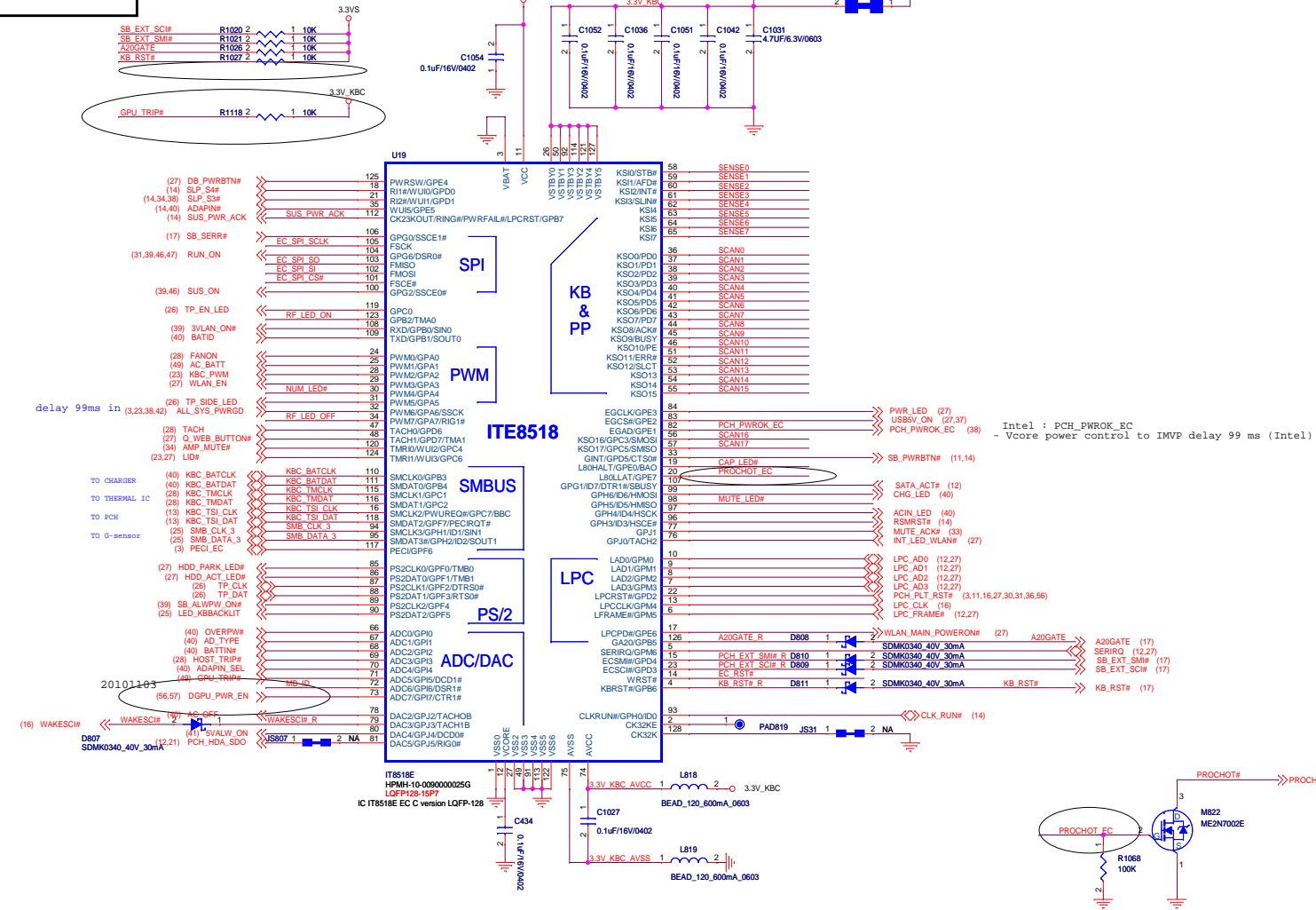
WINBOND	W83L771AWG	ODMH-15-00G0000017G 1001100x(98h)
ON SEMI	ADT7421ARMZ-REEL	???
GMT	G780P81U	???

FAN CONN

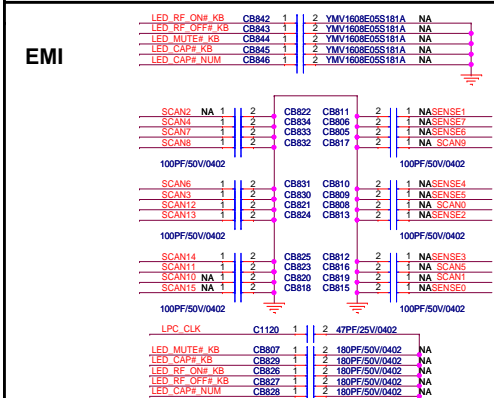
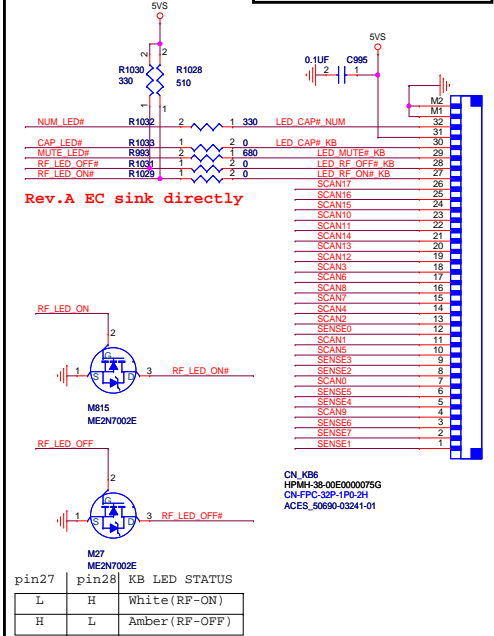


FLEXComputing			
Project Name : H710D11		Title : THERM IC_FAN	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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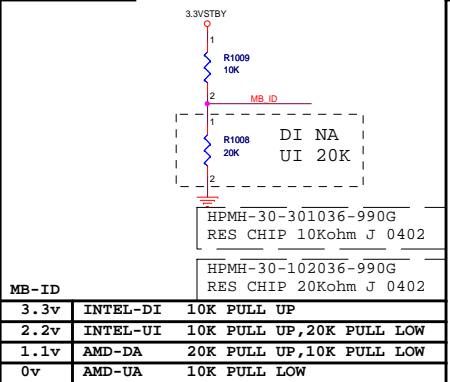
KBC
ITE8518



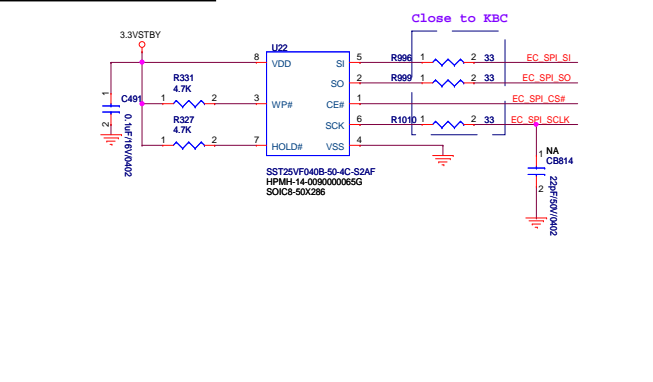
Keyboard Connector



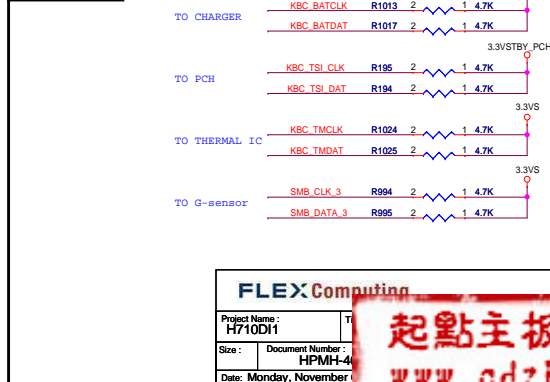
Board ID



SPI ROM (512KB)



SM BUS



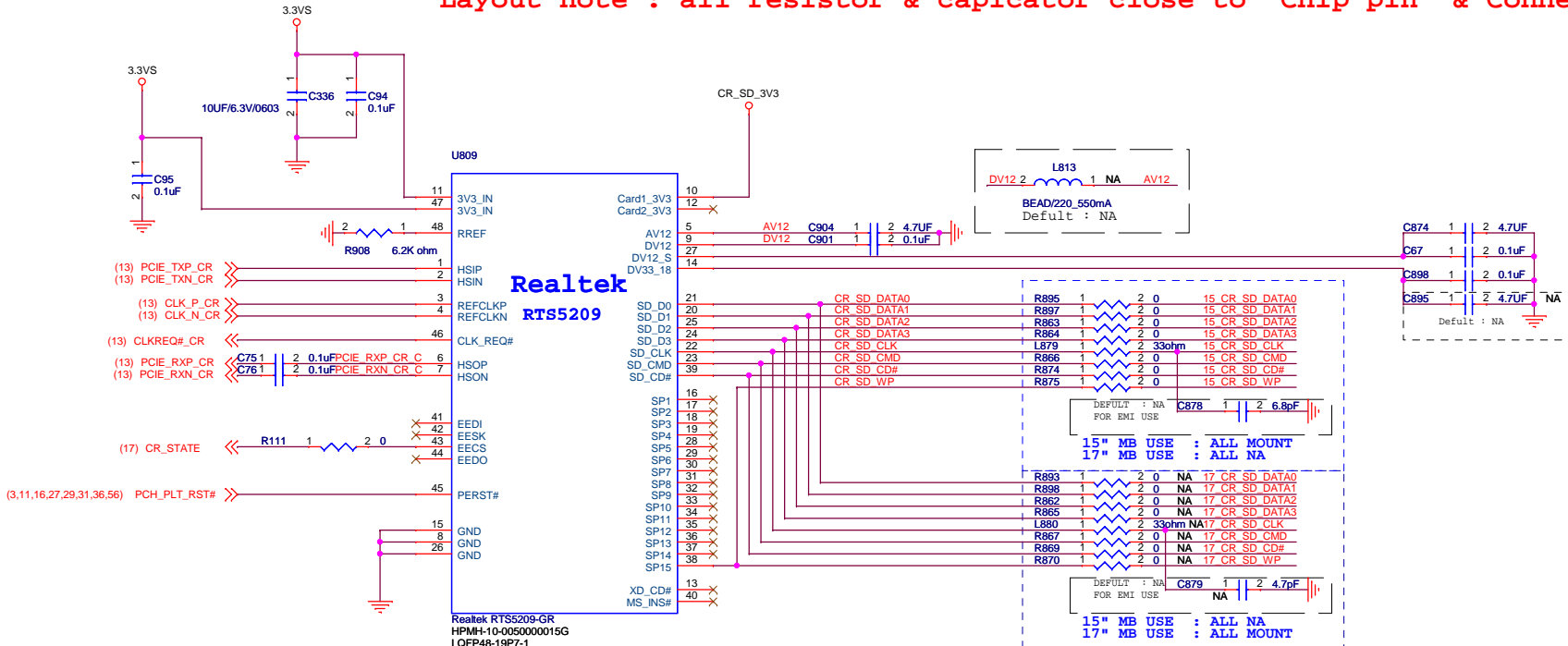
FLEX Computing

Project Name:	H710DI1
Size:	Document Number: HPMH-4
Date:	Monday, November

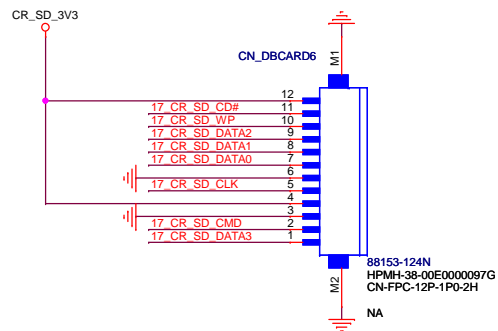
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Card Reader

Layout note : all resistor & capacitor close to Chip pin & Connector pin



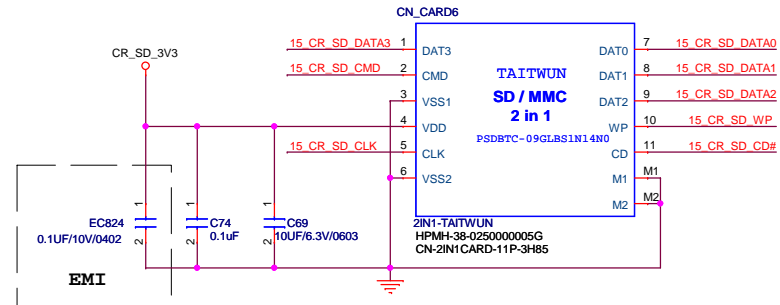
FOR 17" MB USE WTB CONNECTOR



FOR 15" MB ALL COMPONENT : NA

FOR 17" MB ALL COMPONENT : MOUNT

FOR 15" MB USE CardReader CONNECTOR



FOR 15" MB ALL COMPONENT : MOUNT

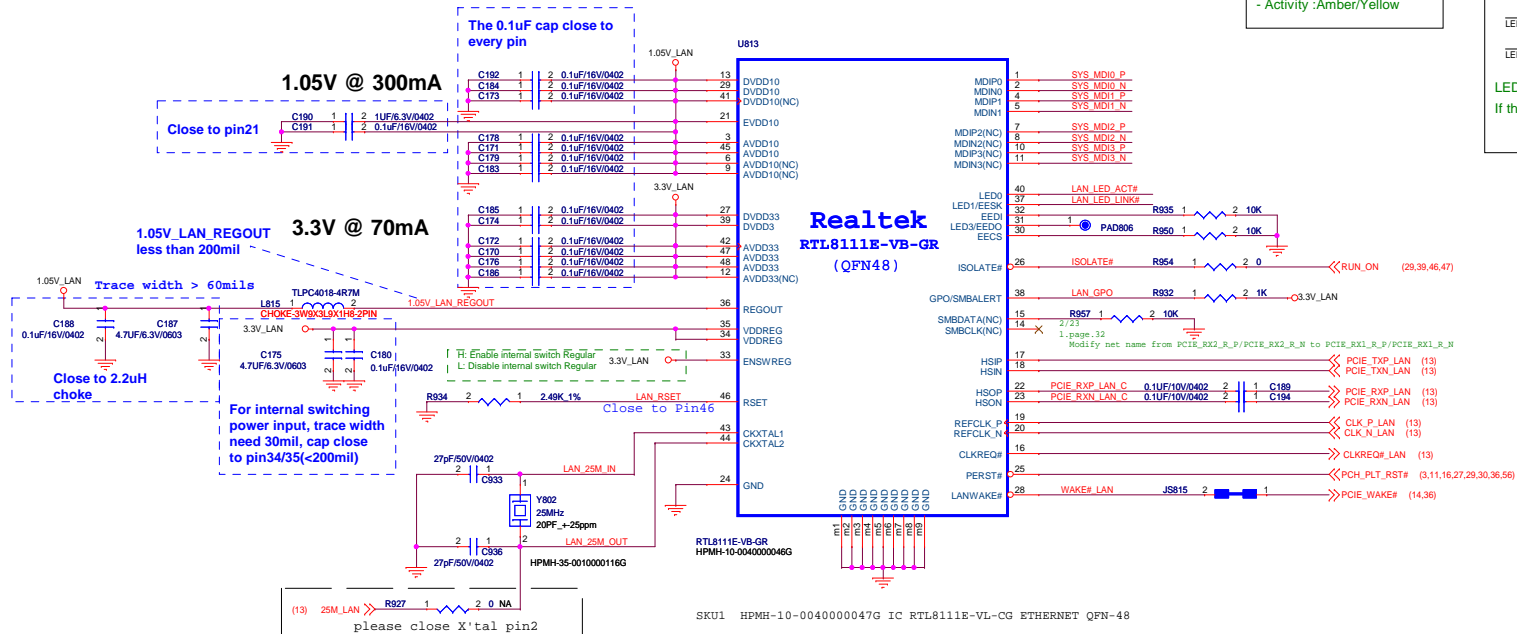
FOR 17" MB ALL COMPONENT : NA

FLEX Computing

Project Name : H710DI1		Title : Card R
Size :	Document Number : HPMH-40GAB660	
Date: Monday, November 08, 2010		

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Gbit LAN Controller

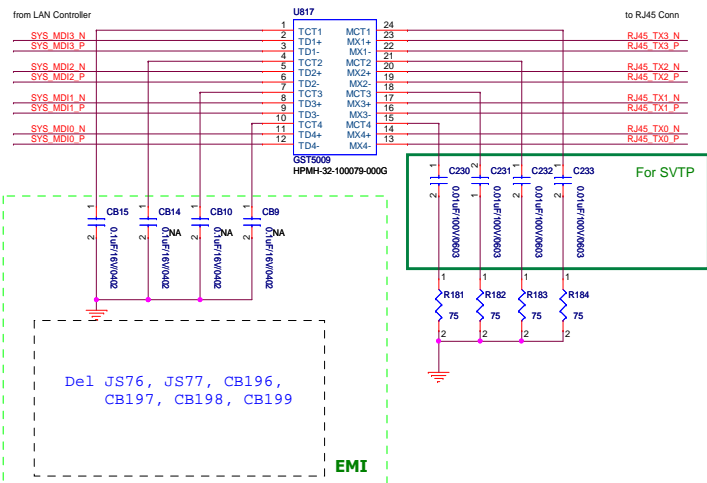


TRANSFORMER

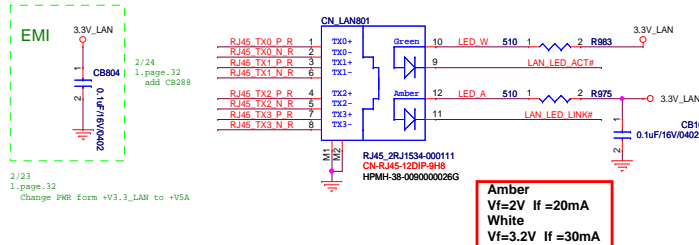
2009.09.22 ref. "RTL8102E_8111D 48PIN demo_board v200_2008.04.30"

Transformer :
Gbit P/N: 32-100079-000G(GST5009)
10/100 P/N: 32-0000000009G (TST1284)

Layout near RJ45 Connector



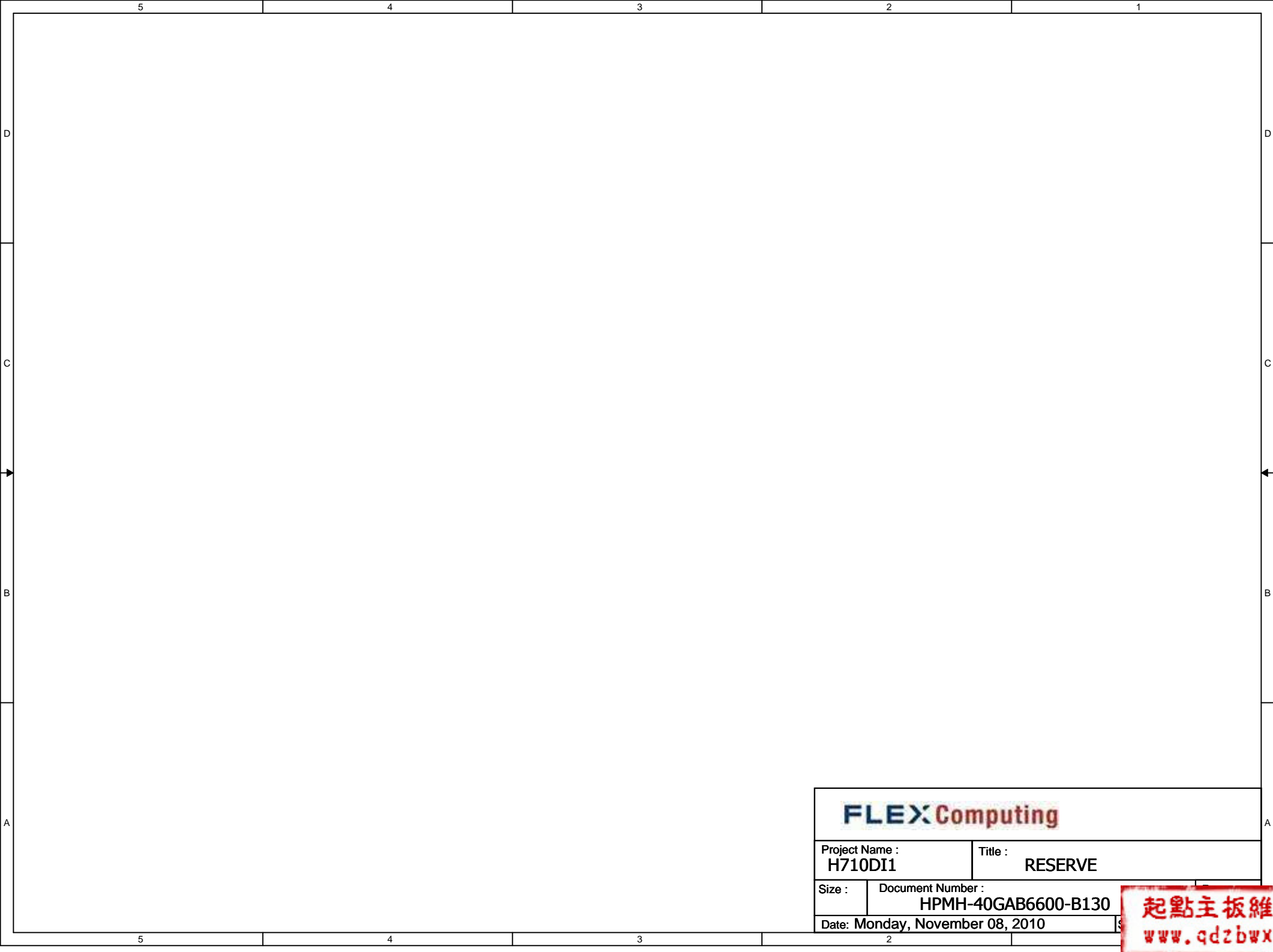
RJ45 Cable Connector



FLEX Computing

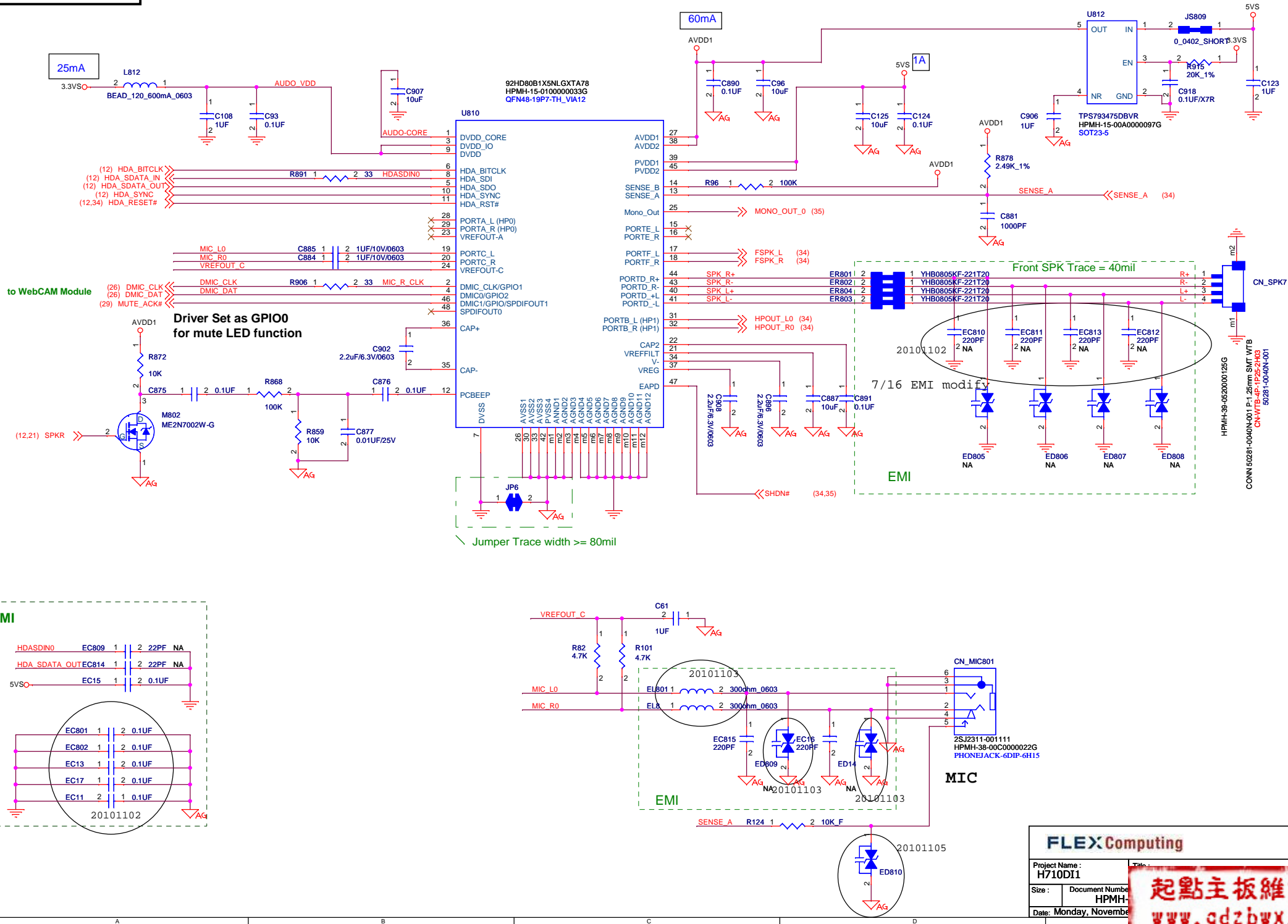
Project Name :
H710DI1
Size :
C Document Number :
HPMH-4
Date : Monday, November

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FLEX Computing	
Project Name : H710DI1	Title : RESERVE
Size :	Document Number : HPMH-40GAB6600-B130
Date: Monday, November 08, 2010	

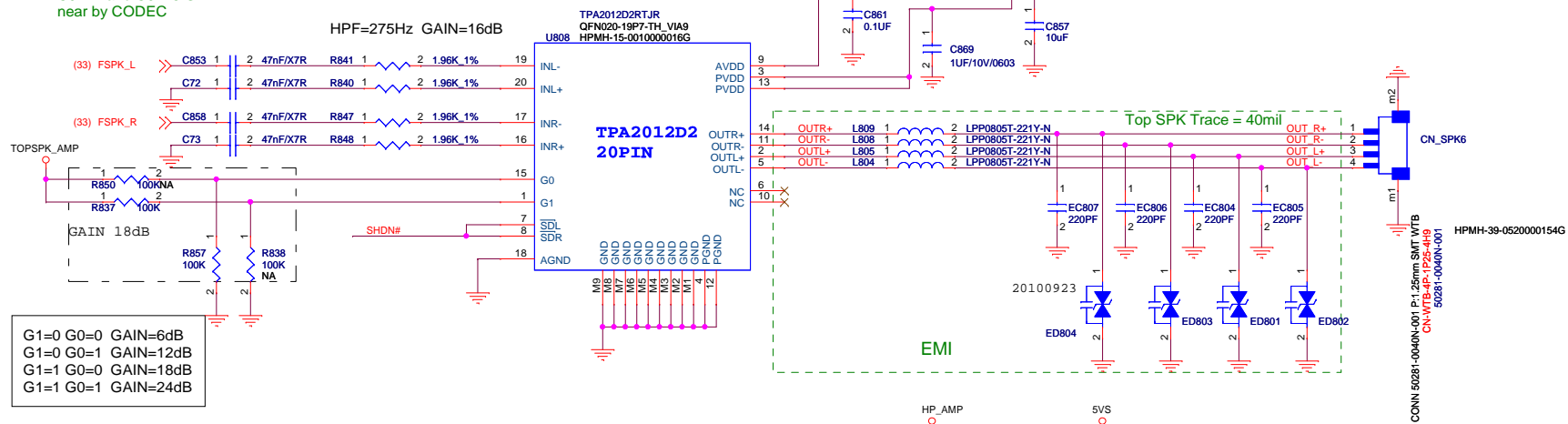
Audio CODEC



C9722 and C9725 GND
near by CODEC

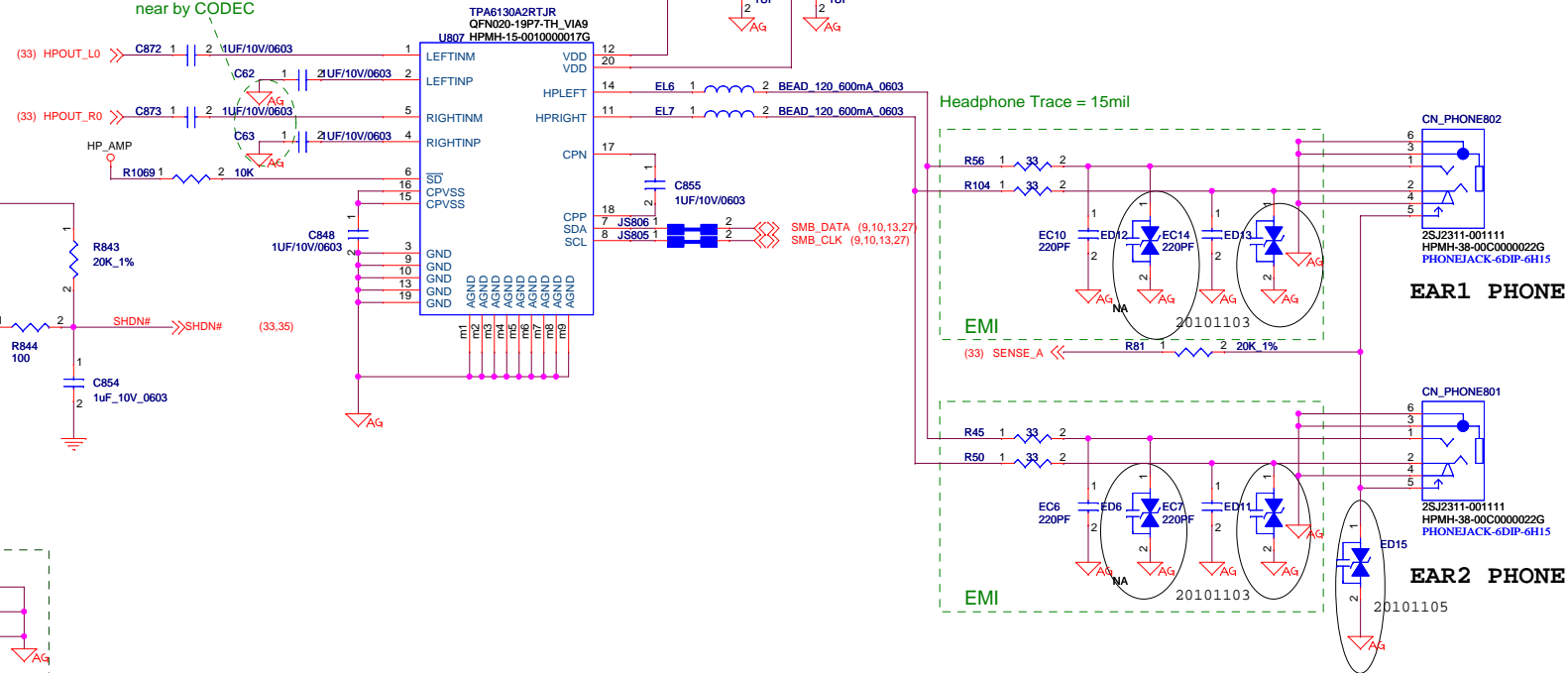
HPF=275Hz GAIN=16dB

Front Speaker AMP



Headphone AMP

C11001 and C11002 AGND
near by CODEC



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Project Name :	H710D11	Title :	Audio 2/3 SPK AMP
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If without supply Woofer all page NA

WOOFER AMP

HPA00836PWPR
HTSSOP28-25P6X220-TH

HPA00836PWPR
28PIN

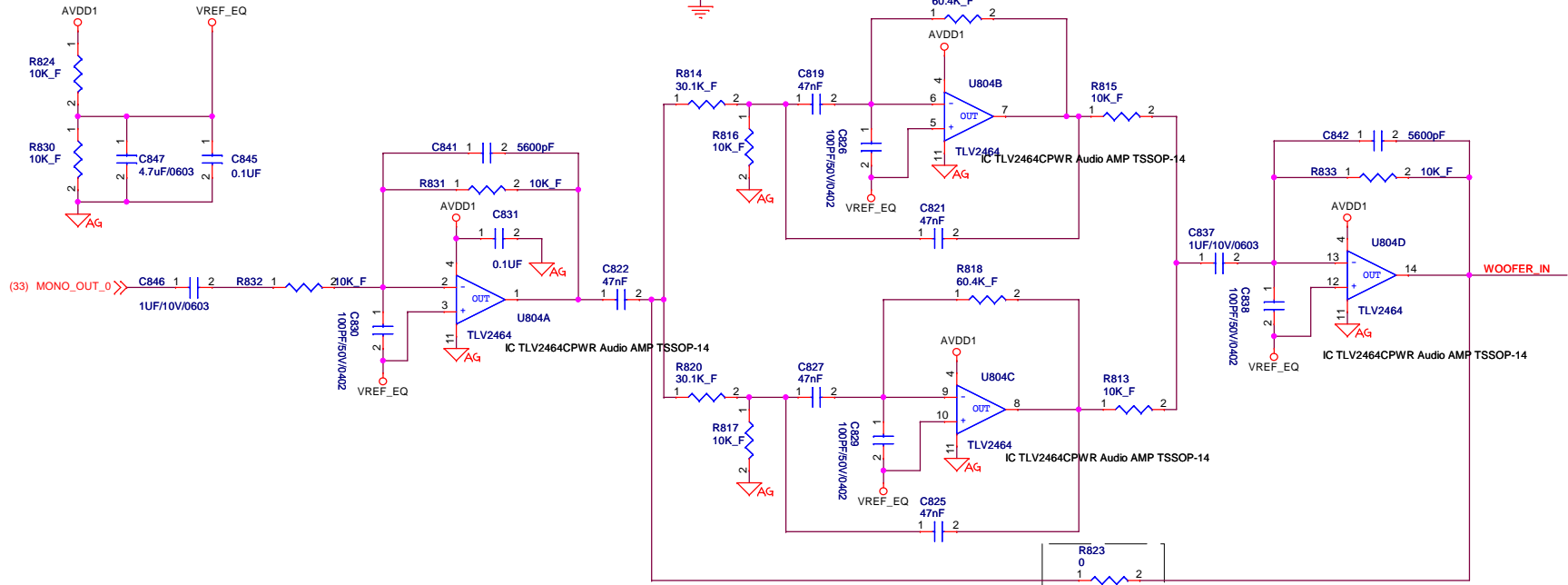
C9742 GND
near by CODEC

5VS

GAIN 20dB

G1=0 G0=0 GAIN=20dB
G1=0 G0=1 GAIN=26dB
G1=1 G0=0 GAIN=32dB
G1=1 G0=1 GAIN=36dB

Kevin modify-0909



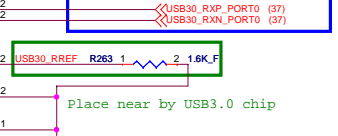
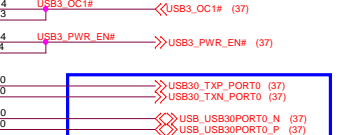
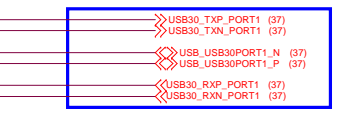
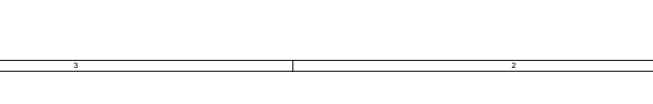
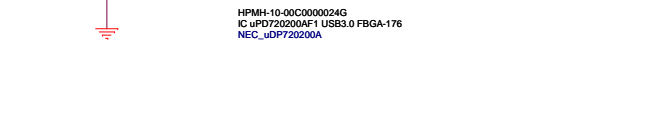
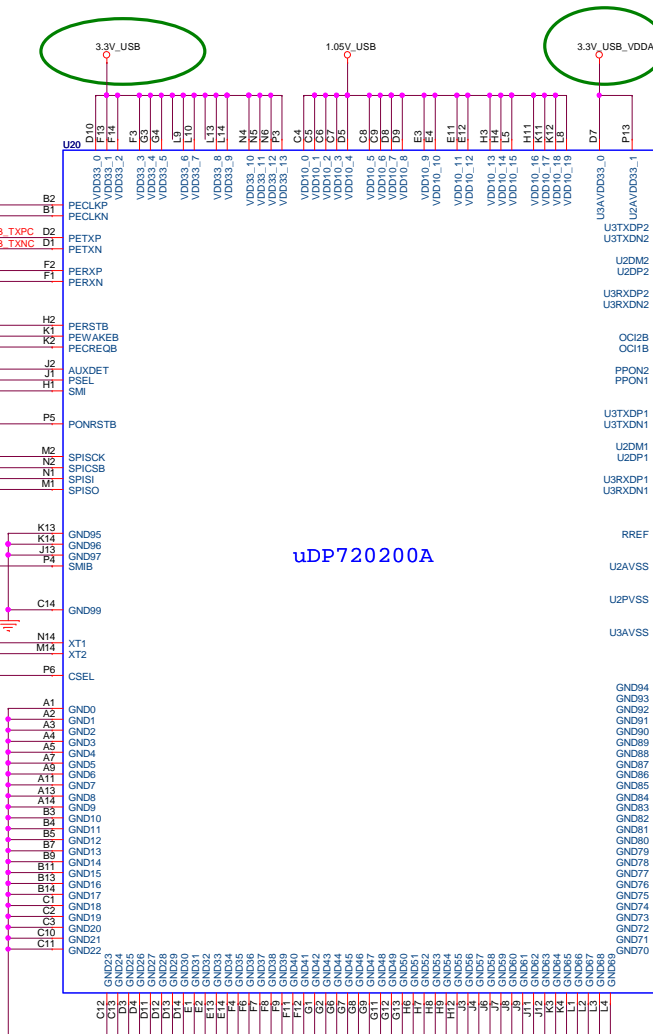
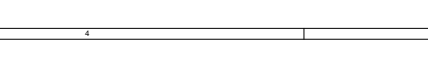
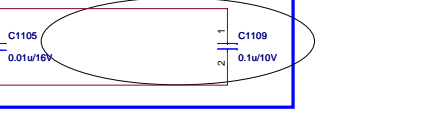
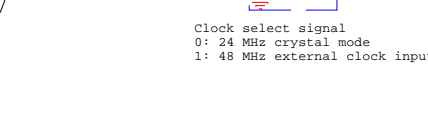
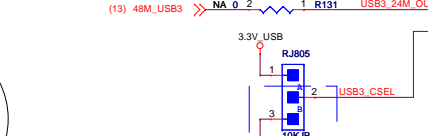
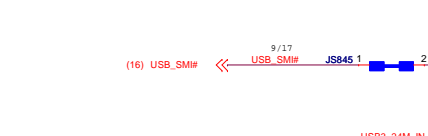
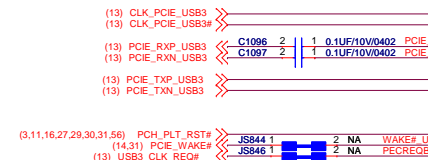
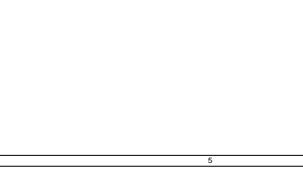
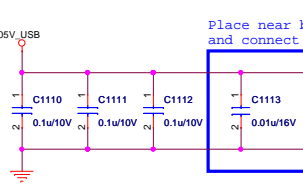
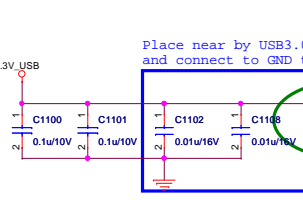
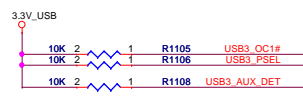
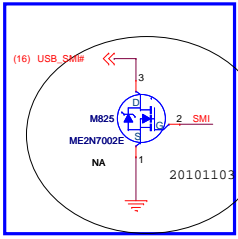
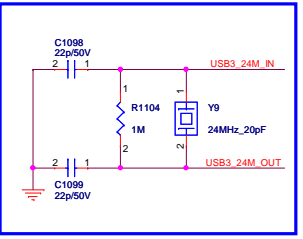
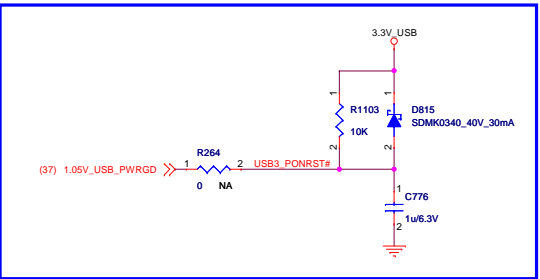
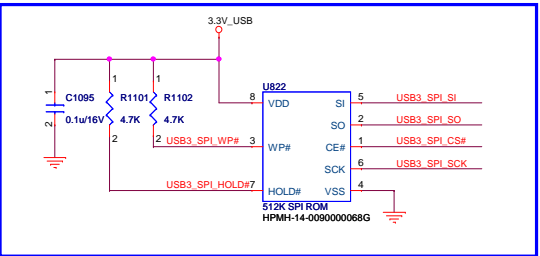
NA
Always NA

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Project Name:	H710DI1	Title:	Audio 3/3 WOOFER AMP
Size:	Document Number:	Rev:	B
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USB3.0 NEC uDP720200



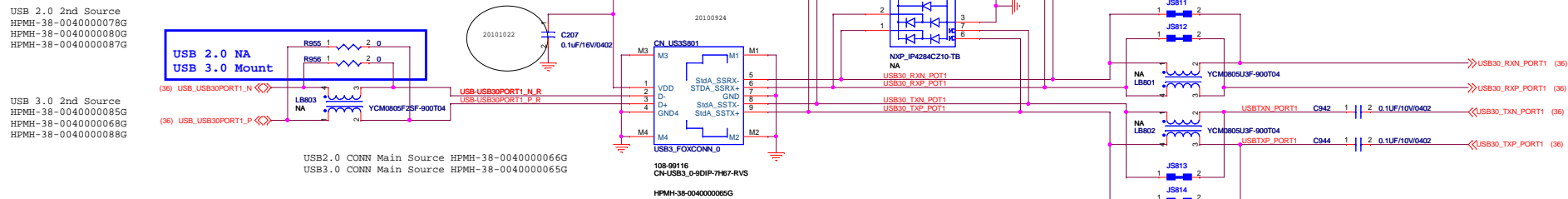
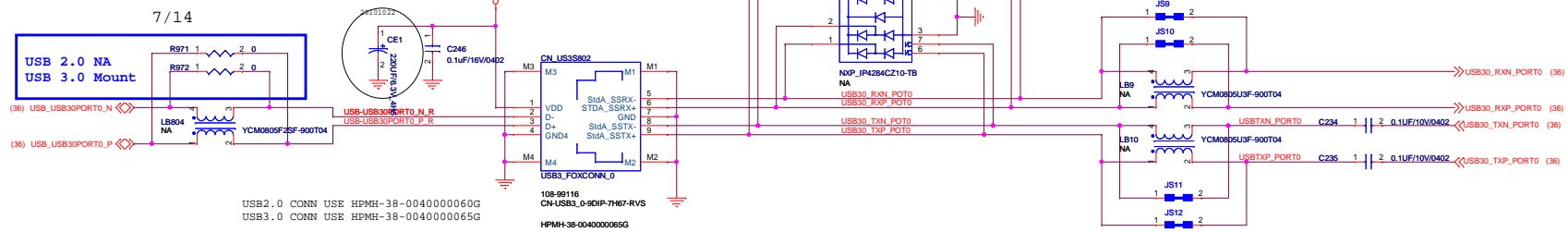
FLEX Computing

Project Name: H7

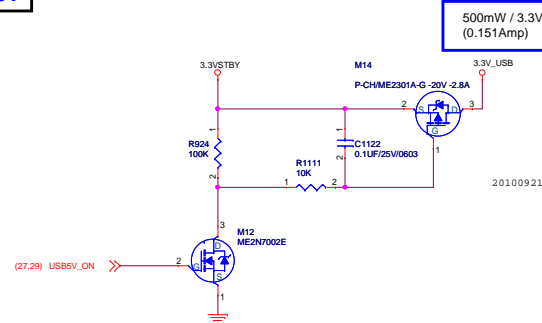
Size: 1

Date: M

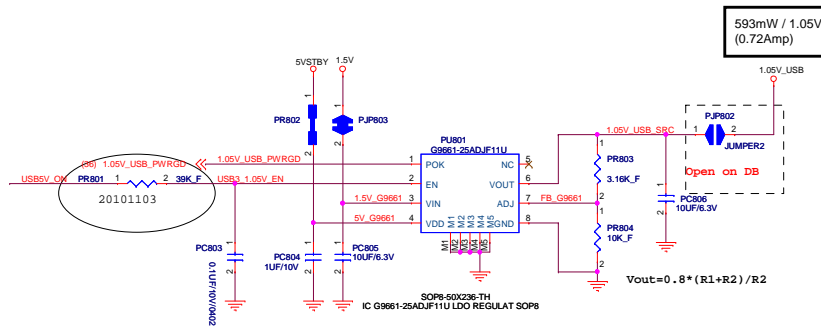
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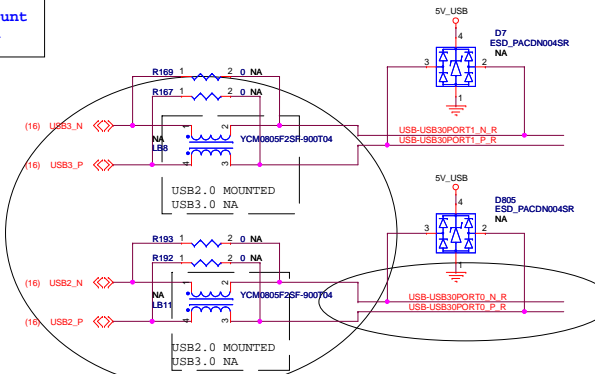
USB3.0 3.3V



USB3.0 1.05V_USB



USB 2.0 Mount USB 3.0 NA



USB POWER SW

7/14 for USB3.0 and USB 2.0

7/14 USB 3.0 mount B
USB 2.0 mount B

(36) USB3_PWR_ENH

(27,29) USB5V_ON

Don't delete this pull-down resistor for disable Power SW in G3.

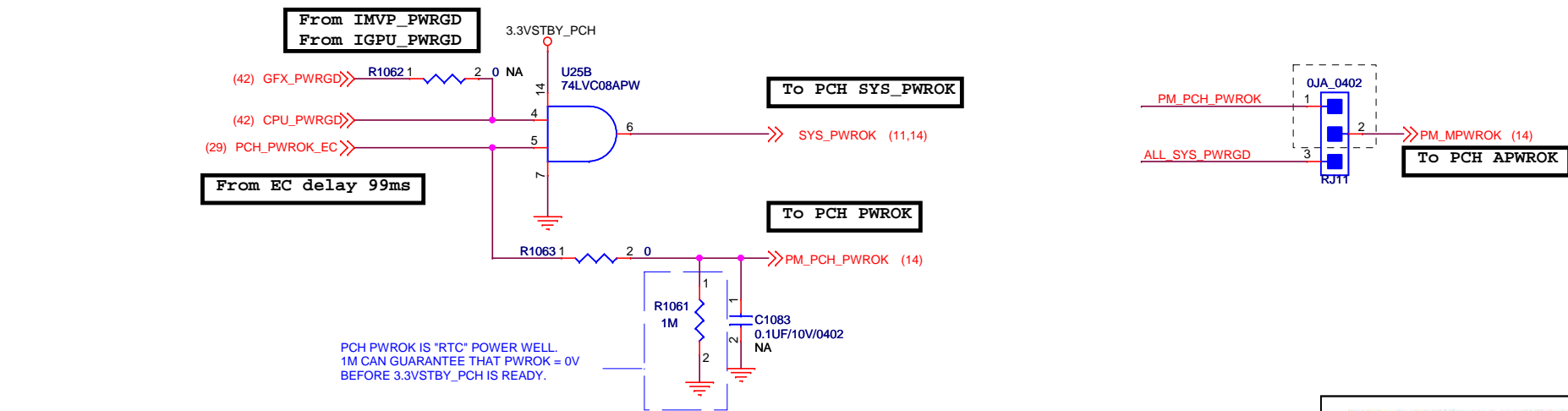
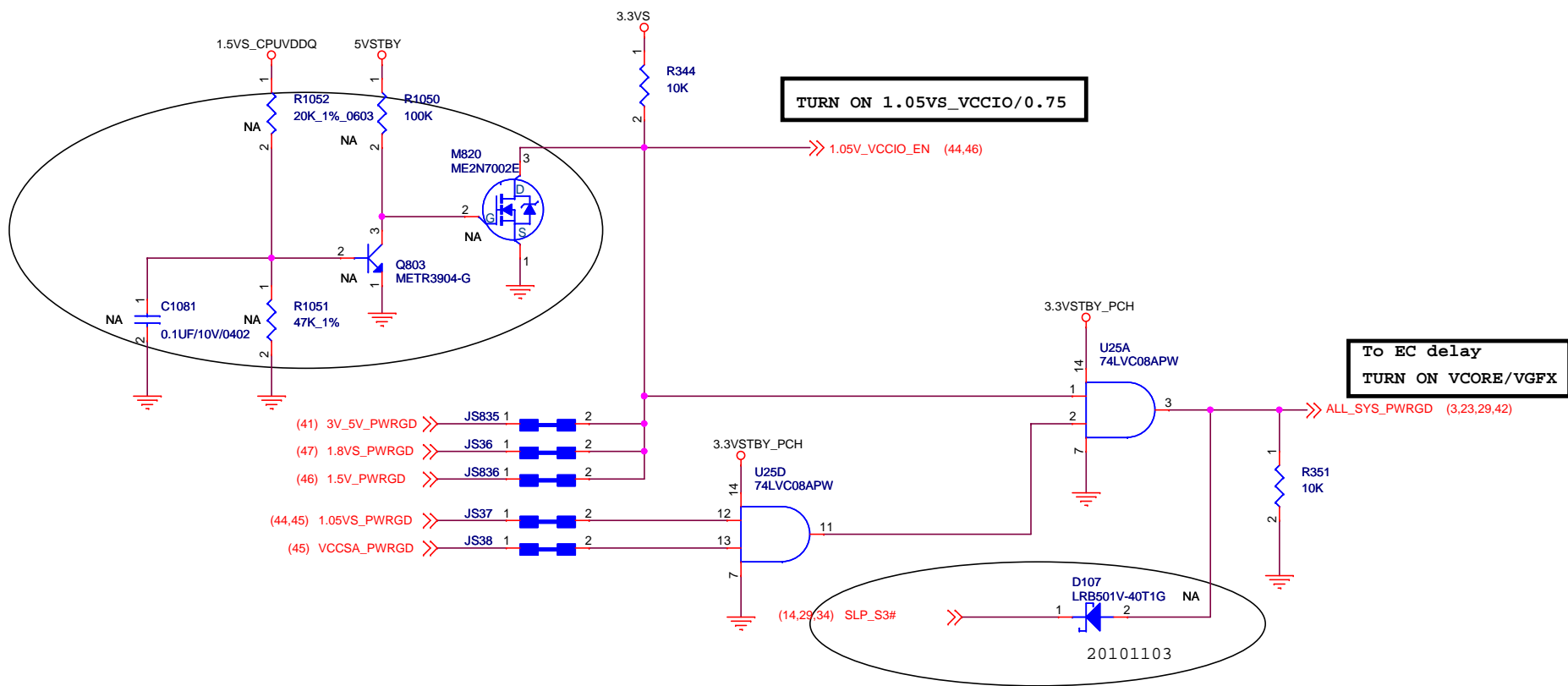
7/14 for USB3.0 (A) and USB 2.0 (B)

FLEX Computing

Project Name : H710D11

Size : HPMH-40GAB6600-B130

Date : Monday, November 08, 2010

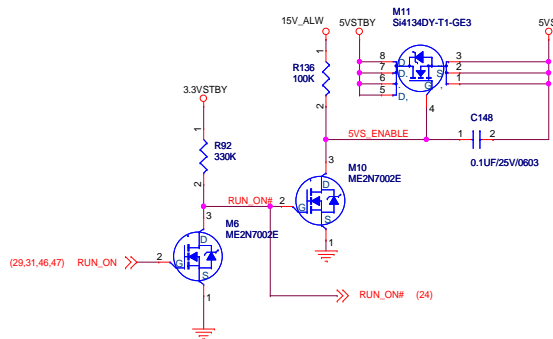


PCH PWROK IS "RTC" POWER WELL.
1M CAN GUARANTEE THAT PWROK = 0V
BEFORE 3.3VSTBY_PCH IS READY.

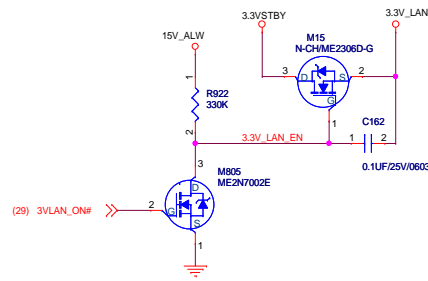
FLEXComputing

Project Name : H710D11		Title : POW...
Size : Custom	Document Number : HPMH-40GAB6	
Date: Monday, November 08, 2010		

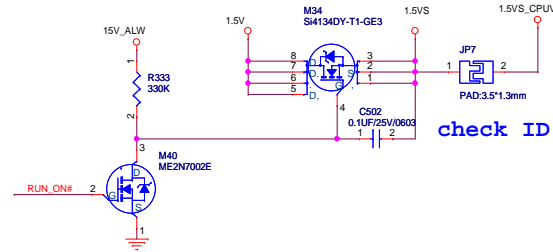
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TDC: ?A



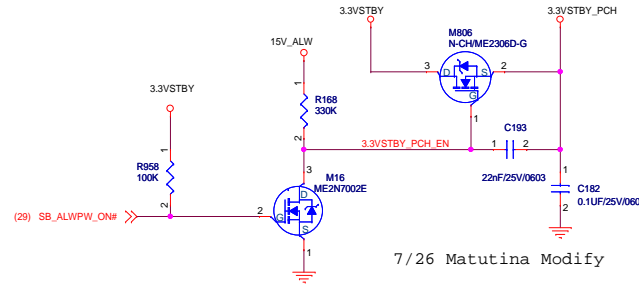
TDC: 0.3A



TDC: ?A

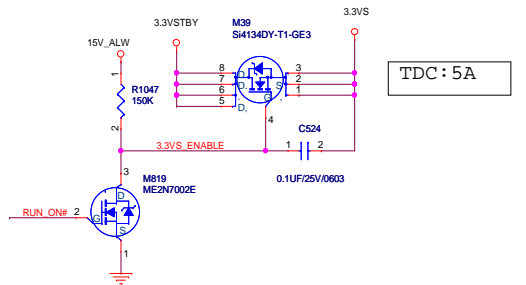
check ID

ME4626 :
Vgs(th): 3V(max)
Rds(on): 3.2m@Vgs = 10V (Max)
Rds(on): 4.9m@Vgs = 4.5V (Max)
Id : 23A



TDC: 0.6A

7/26 Matutina Modify



TDC: 5A

ME2306D:

Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 31m@Vgs = 10V(MAX)
Rds(on) : 52m@Vgs = 4.5V(MAX)
Id : 3.9A(Max)

ME4894-G:

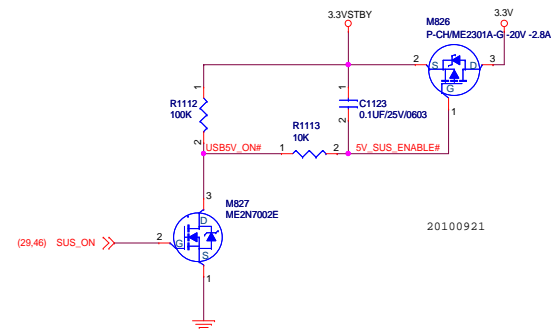
Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 11.7m@Vgs = 10V (MAX)
Rds(on) : 18.2m@Vgs = 4.5V(MAX)
Id : 11.5A(Max)

ME2301A:

Vgs(th) : -0.9V(max)
Rds(on) : 75m@Vgs = -4.5V(MAX)
Id : -2.8A(Max)

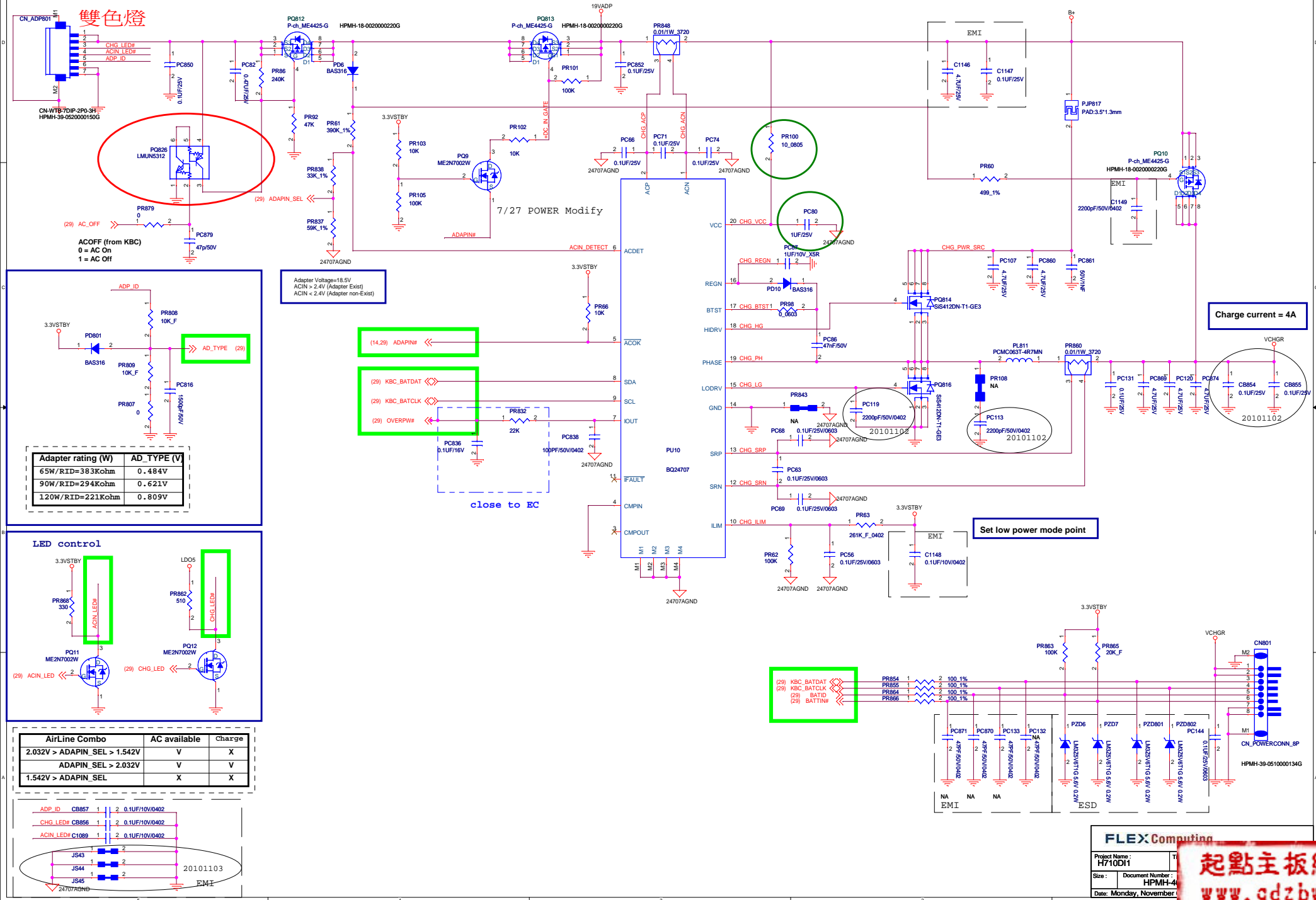
3.3V

500mW / 3.3V



20100921

Charger



5V / 3.3VSTBY

Freq=300KHz
TDC = 7 A
OCP = 10 A

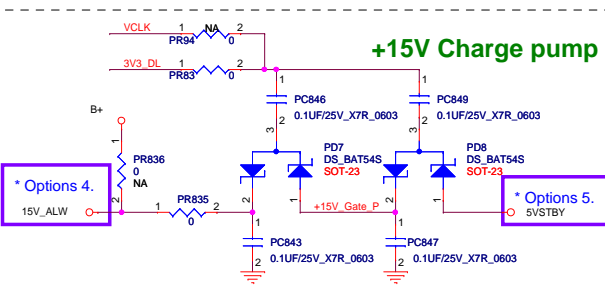
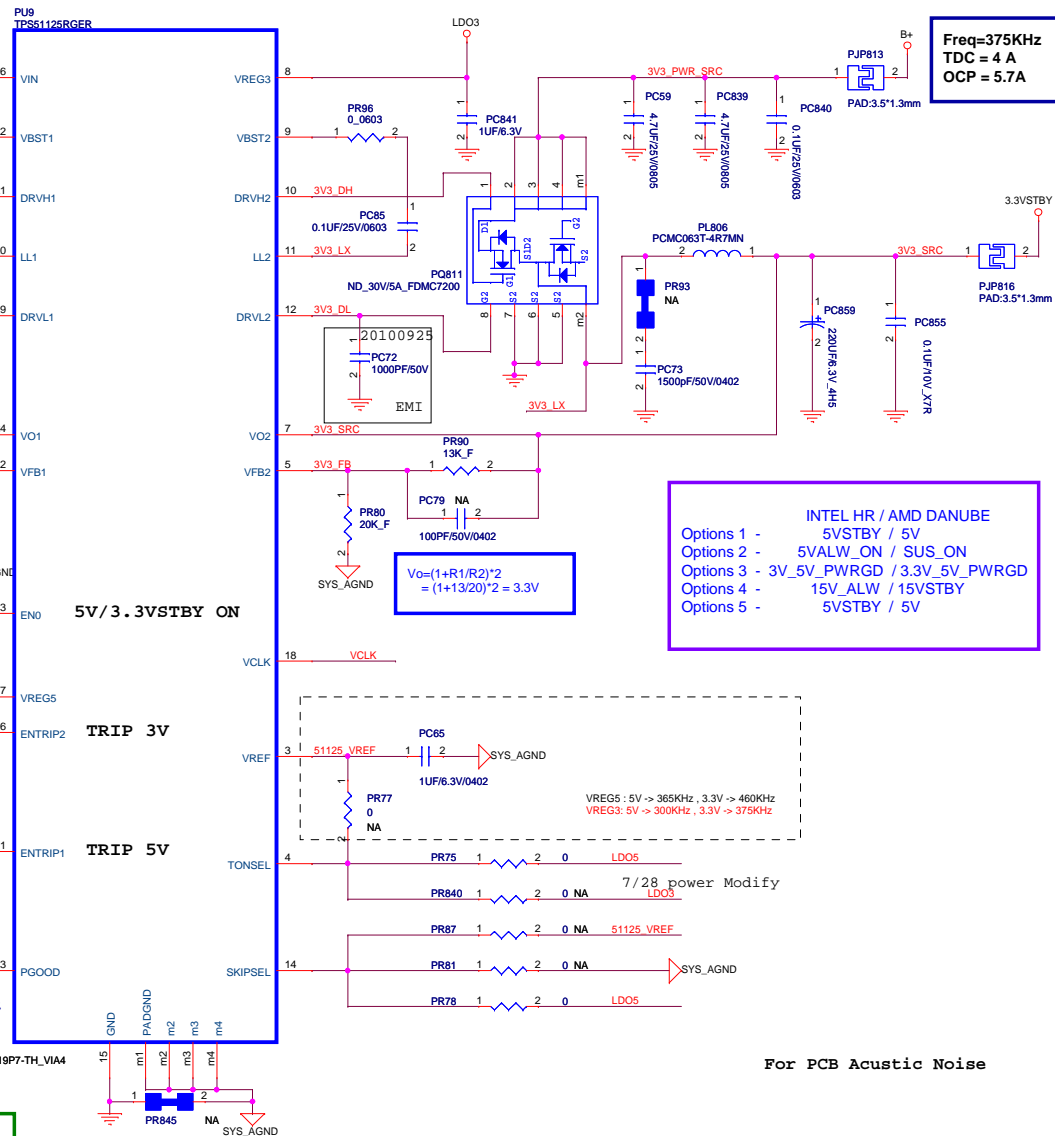
* Options 1.
5VSTBY

* Options 2.

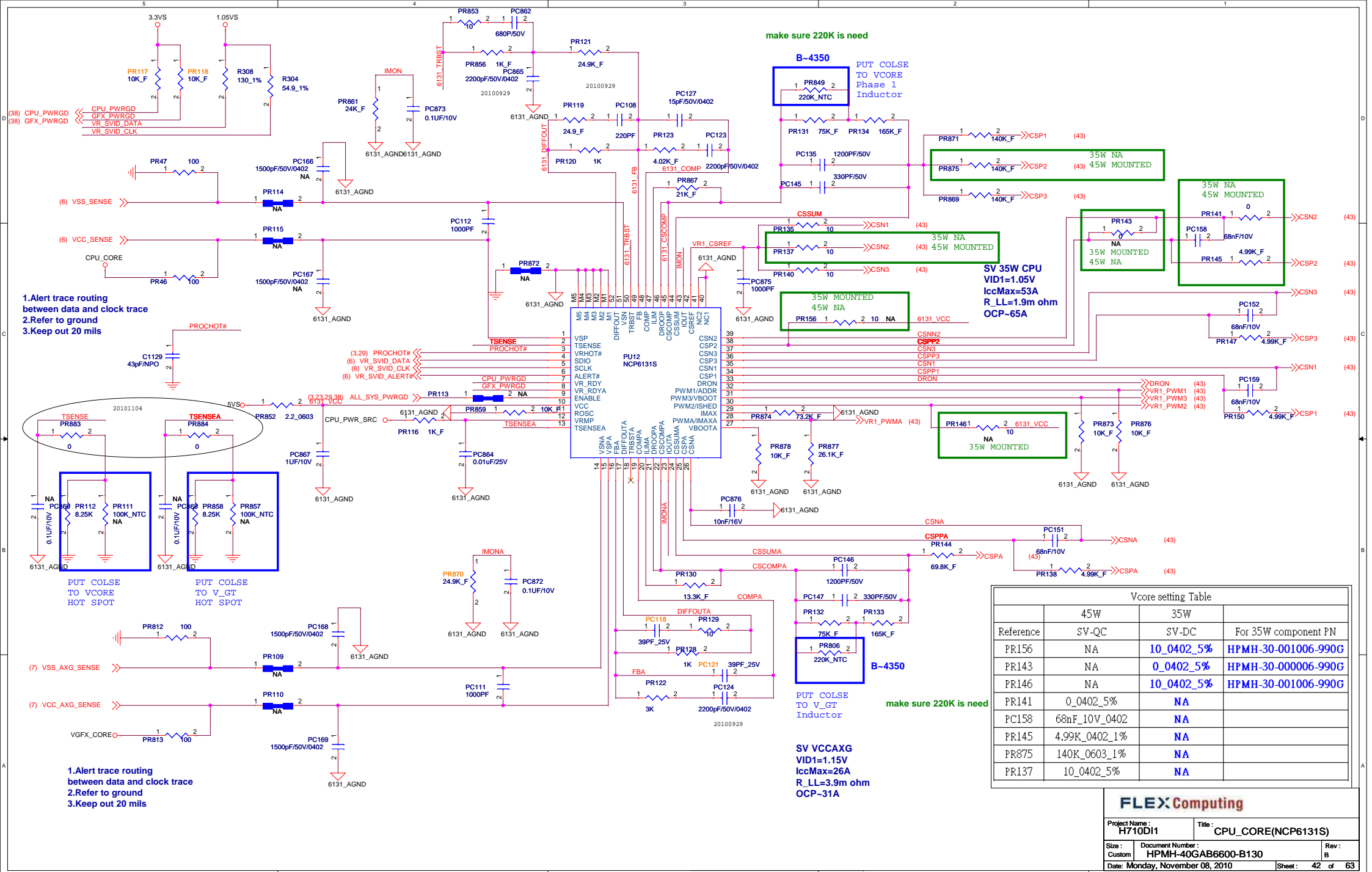
Table 3. Enabling State

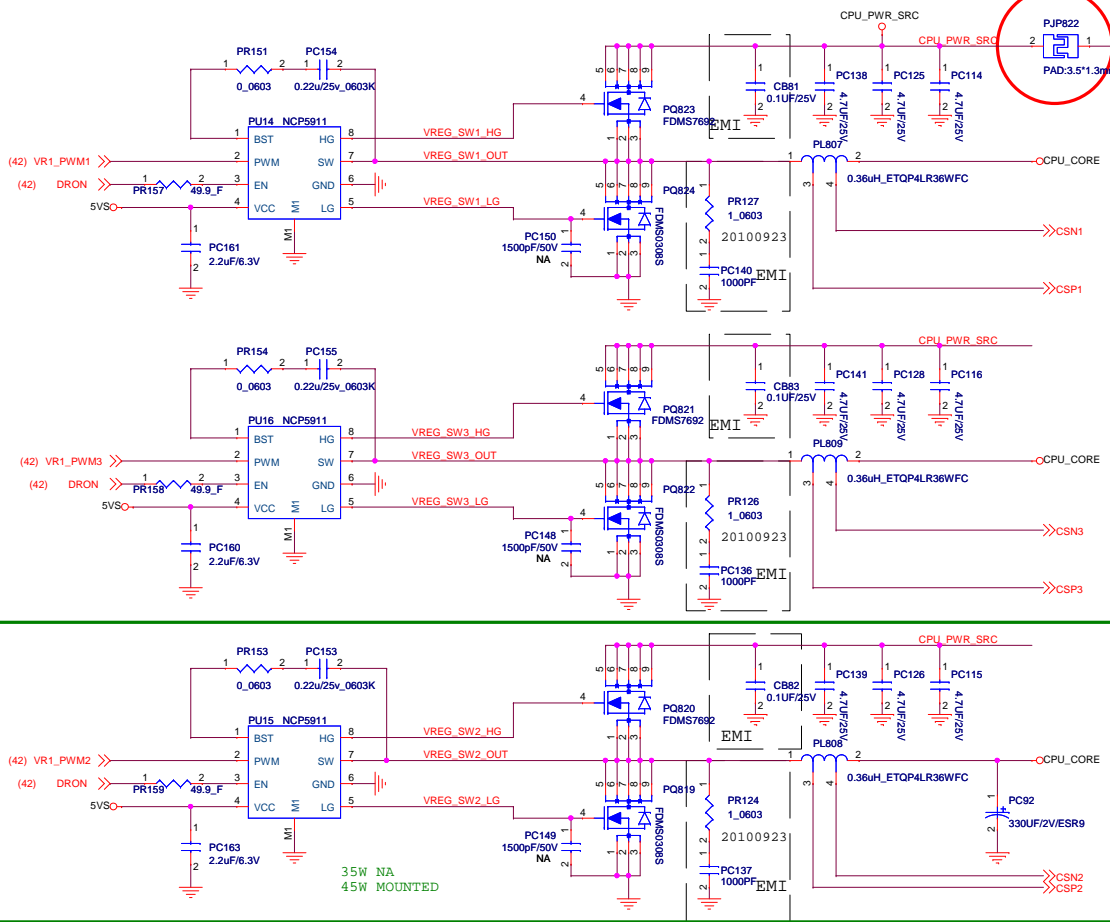
EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	Off

PU3-m1
For layout request, no connect anything.



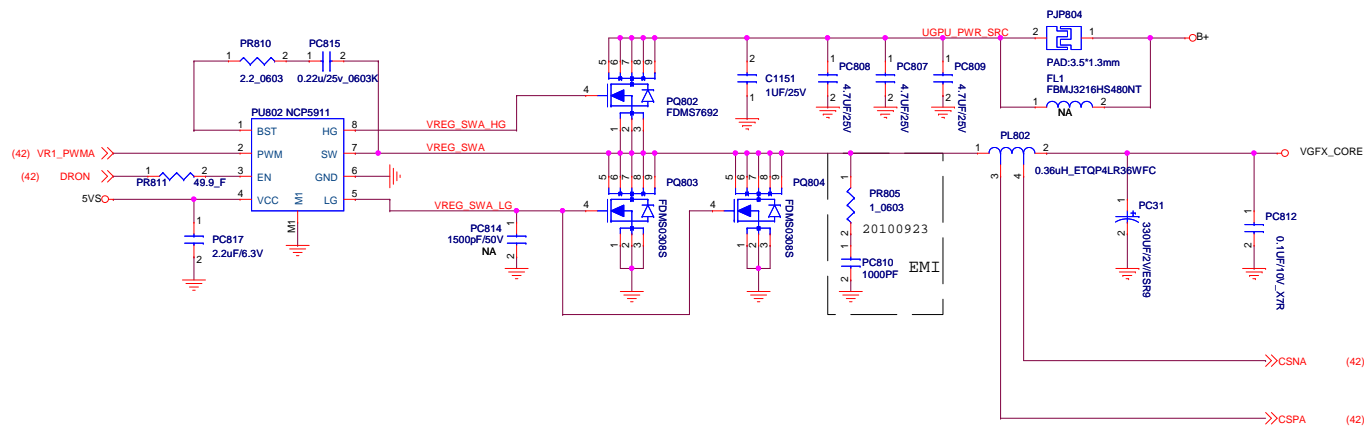
INTEL HR / AMD DANUBE
Options 1 - 5VSTBY / 5V
Options 2 - 5VALW_ON / SUS_ON
Options 3 - 3V_5V_PWRGD / 3.3V_5V_PWRGD
Options 4 - 15V_ALW / 15VSTBY
Options 5 - 5VSTBY / 5V





Vcore setting Table

	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PU15	NCP5911	NA	
PR153	0_0603_5%	NA	
PC153	0.22UF_25V_0603	NA	
PR159	49.9_0402_1%	NA	
PC163	2.2UF_6.3V_0603	NA	
PQ820	FDMS7692	NA	
PQ819	FDMS0308S	NA	
PL808	0.36uH	NA	
PR874	73.2K_0402_1%	41.2K_0402_1%	HPMH-30-141221-990G
PR861	24K_0402_1%	24.9K_0402_1%	HPMH-30-124921-990G
PR867	21K_0402_1%	12.4K_0402_1%	HPMH-30-112421-990G



1.05VS_VCCIO
1.05VS

(38,45) 1.05VS_PWRGD

(38,46) 1.05V_VCCIO_EN

$$I_{OCP} = ((PR4551 * 10) / 8 * R_{ds(on)}) + I_{O(max)} / 6 = 18.4A$$

Freq=430KHz

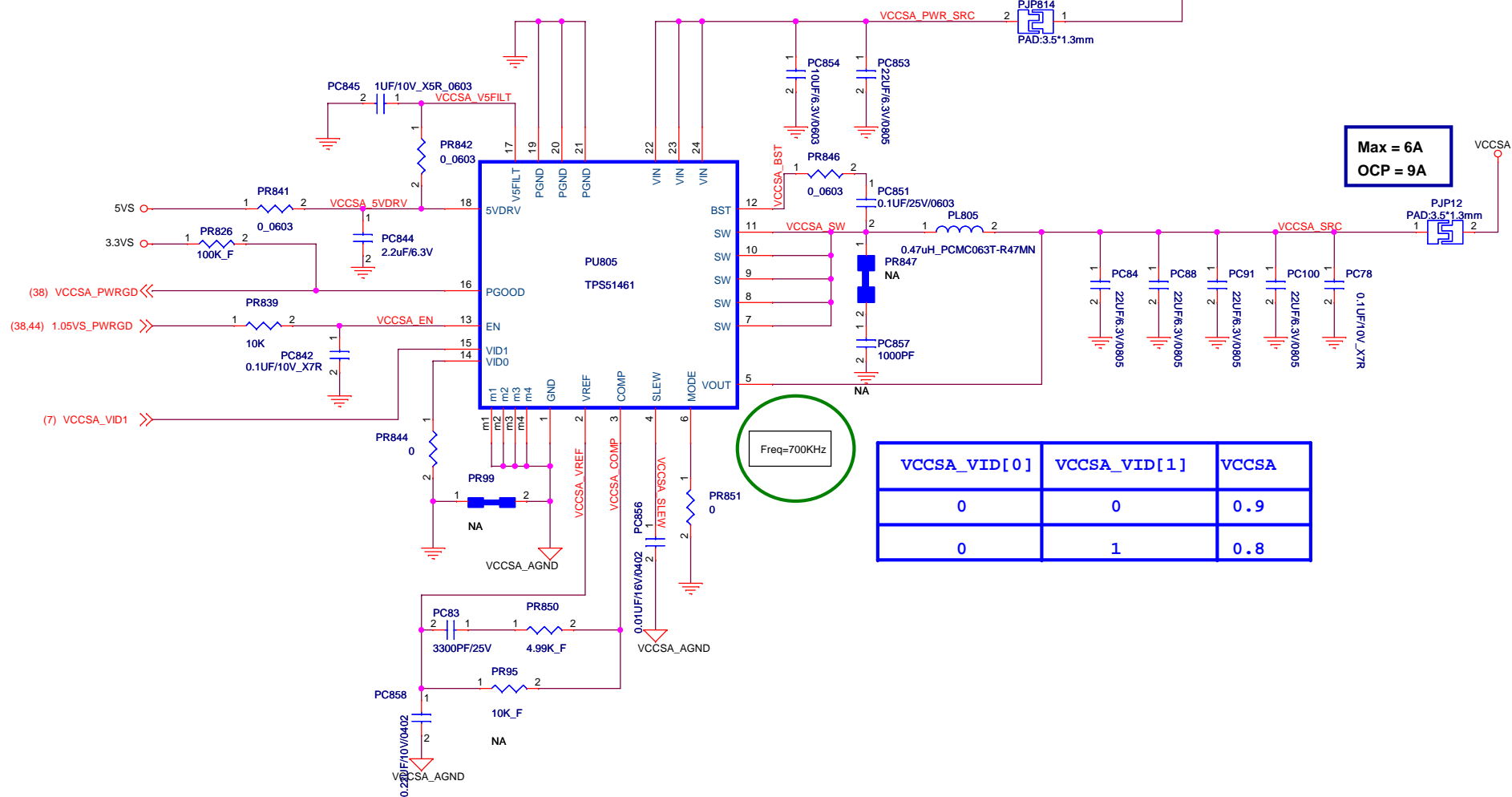
RF pull down to GND with resistor : Auto-skip
RF connect to PGOOD with resistor : Force CCM

$$V_o = 0.75 * (1 + (PR529 / PR531)) = 0.75 * (1 + 0.47) = 1.107V$$

TDC=12.87A
OCP=15.54A

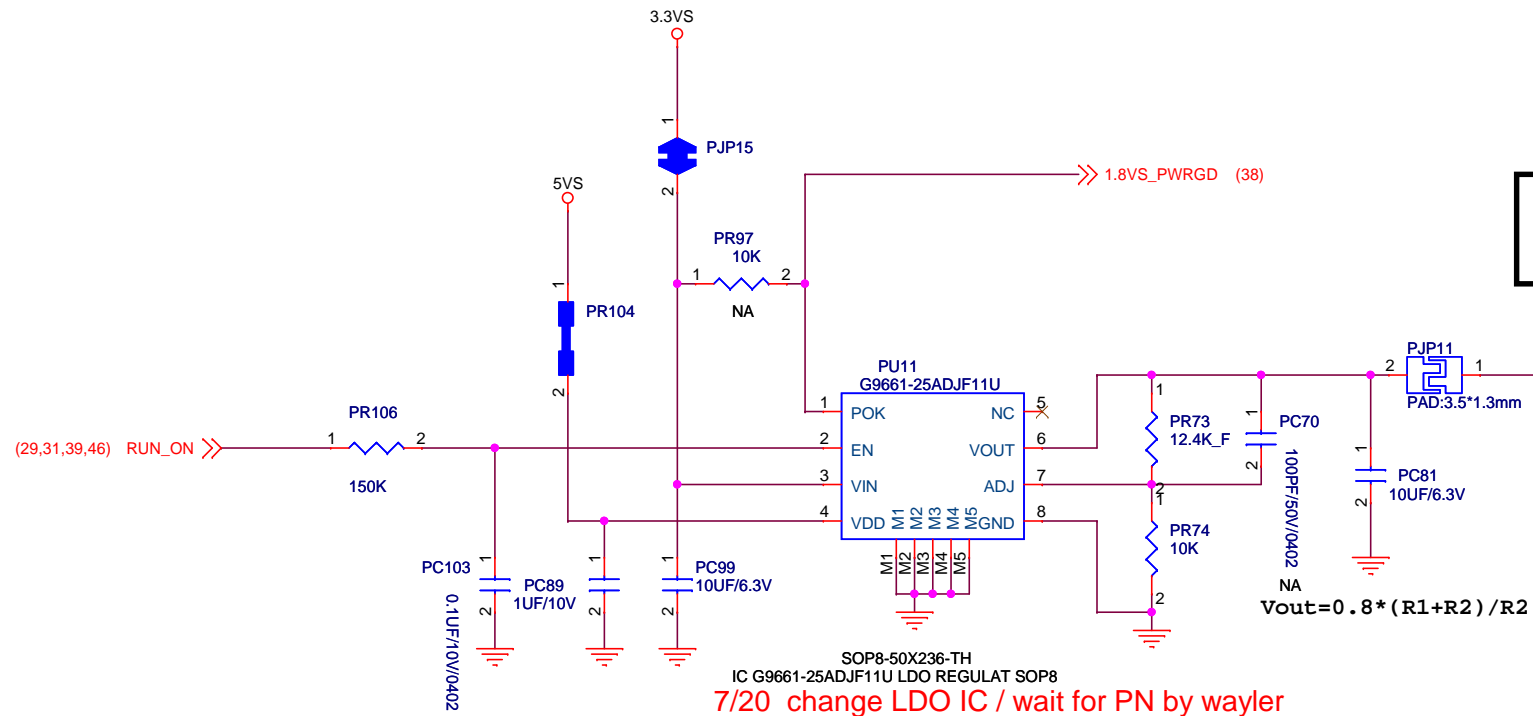
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Project Name : H710DI1		Title : 1.05VS(TPS51218)	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet :	44 of 63

VCCSA


VCCSA_VID[0]	VCCSA_VID[1]	VCCSA
0	0	0.9
0	1	0.8

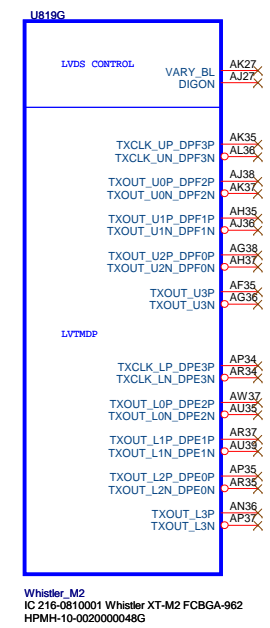
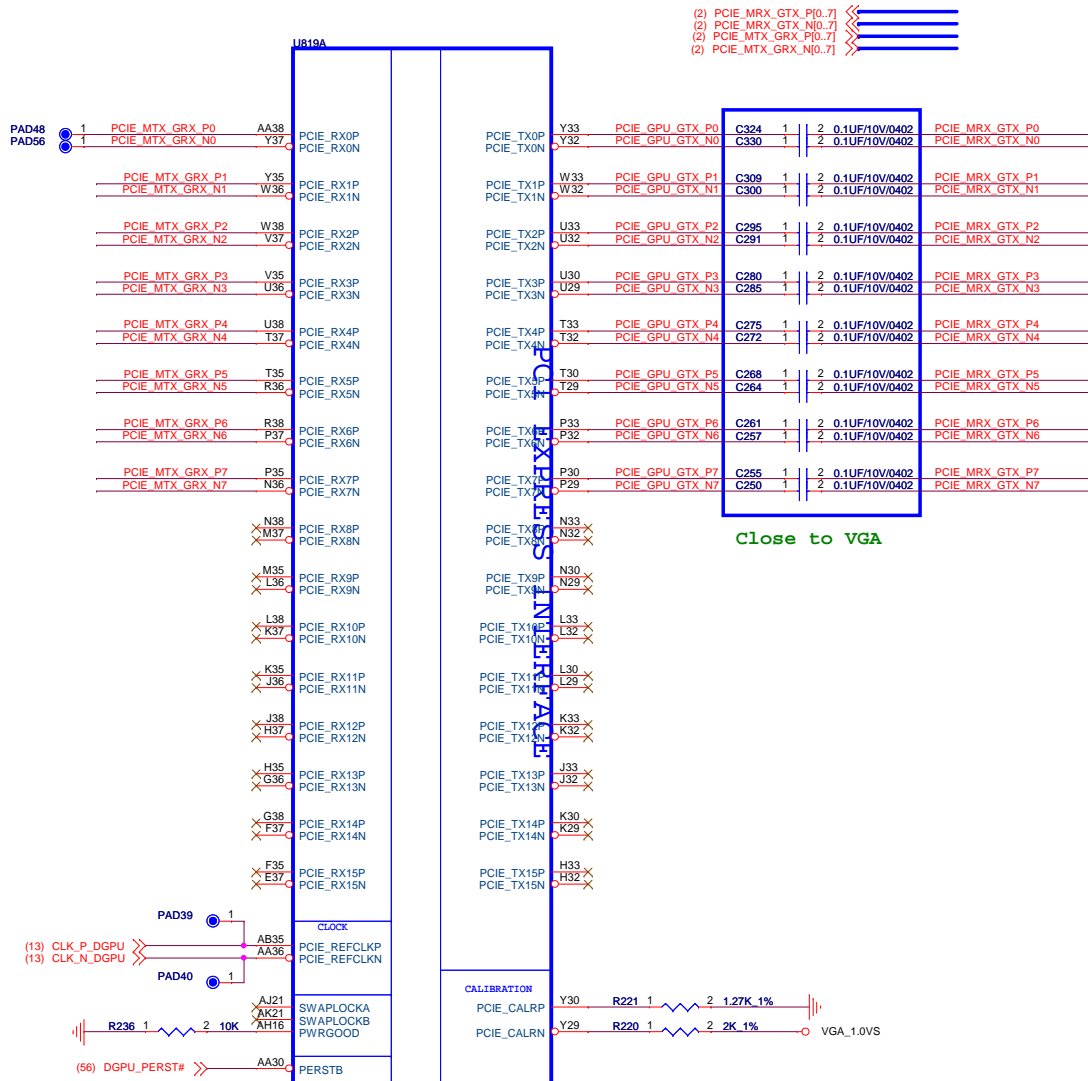
1.8VS



MAX:
UI=1.45A

1.8VS for CPU & PCH

			
Project Name : H710DI1		Title : 1.8VS	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 47 of 63	



GPU TYPE	PN
Whistler XT	HPMH-10-0020000048G
Seymour-XT	HPMH-10-0020000049G

FLEX Computing		
Project Name : H710D11	Title : Capilano_1/5_PCIE/LVDS	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Mon		

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For del vBIOS ROM design:

- 1.P49 -U8,C47,R54
- 2.P53 -R1001,R1002,R1015

For GDDR5 used

VGA, 3.3V/S

UB

VDD

SI

SO

CE#

SCK

HOLD#

VSS

5 DGPU ROMSI

2 DGPU ROMSO

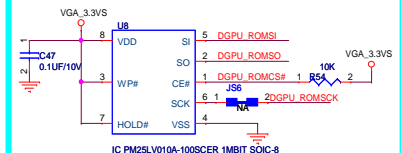
1 DGPU ROMS#

2 DGPU ROMSCK

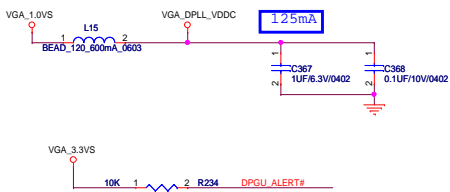
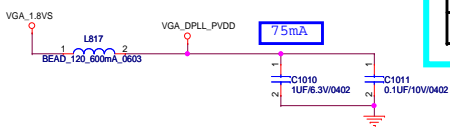
10k

VGA, 3.3V/S

IC PM25LV10A-100SCER 1MBIT SOIC-8



NA for del vBIOS ROM design.



VGA_1.8VS

R1100 10K NA

R1019 10K

R1018 10K NA

VMEM_ID0

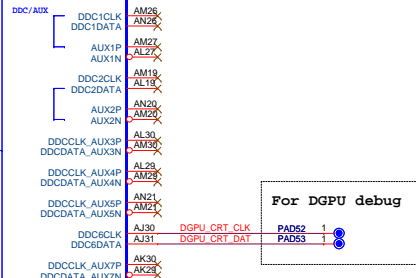
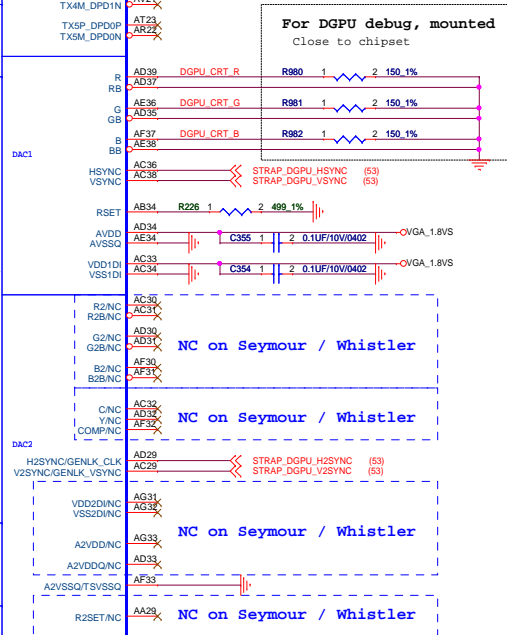
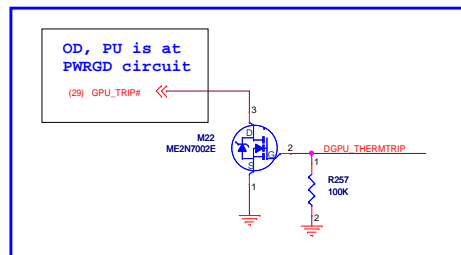
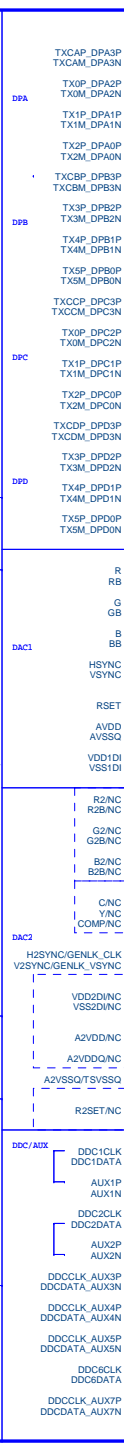
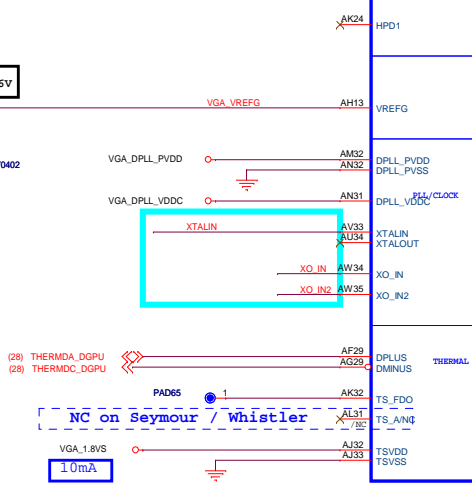
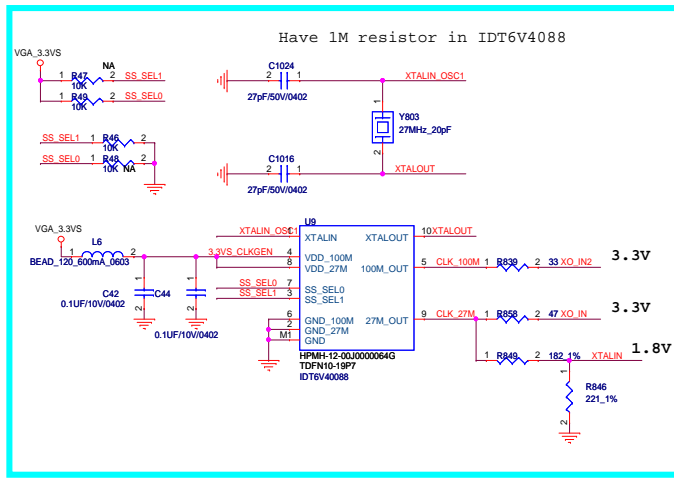
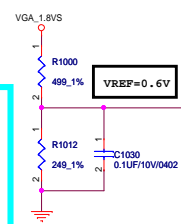
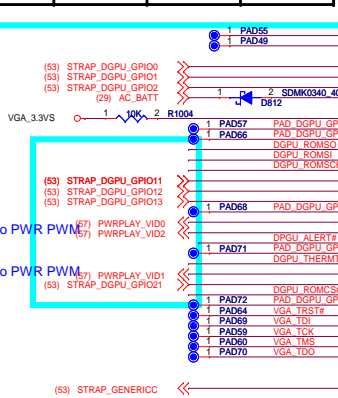
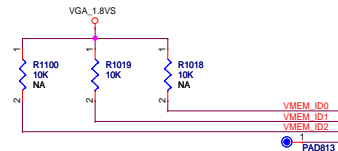
VMEM_ID1

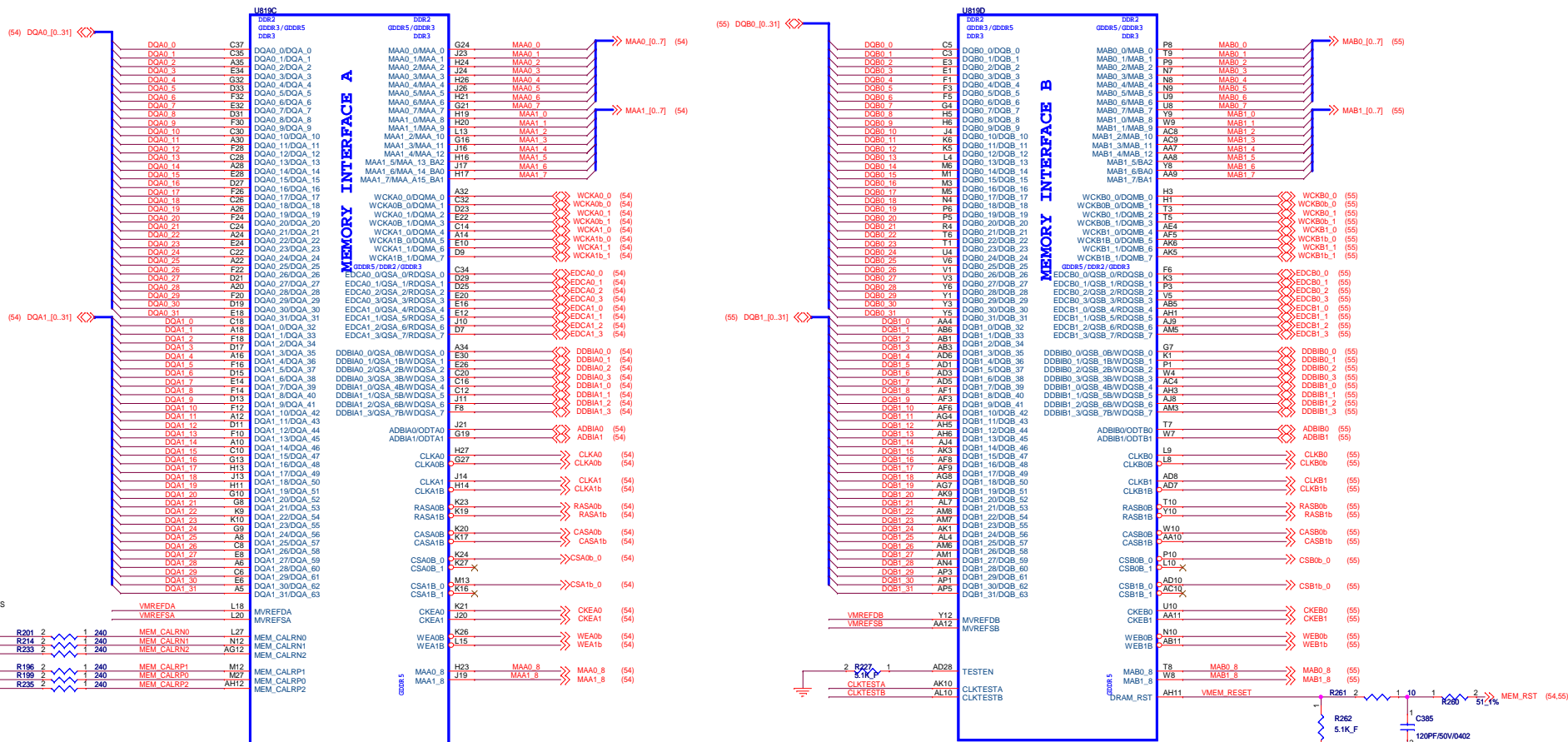
VMEM_ID2

VMEM_ID3

100 MHz Spread Selection Table

PIN3	PIN7	PIN5	
S1	S0	Down	Spread%
L	L	OFF	
L	M	-0.5	
L	H	-2.5	
M	L	-0.25	
M	M	-0.75	
M	H	-1.0	
H	L	-1.5	
H	M	-2.0	Default
H	H	-3.0	

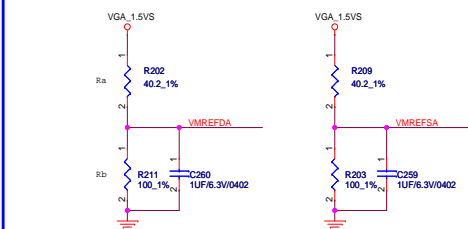




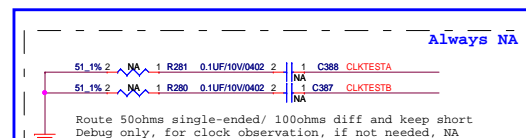
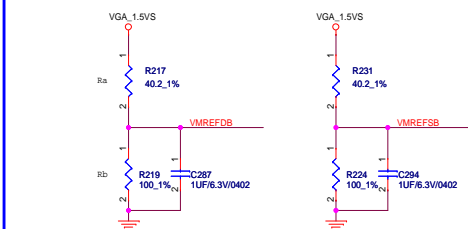
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

VRAM TYPE		PN
Hynix H5GQ1H24AFR-T2C	64MX16(32MX32)	HPMH-14-00300000001G
Hynix H5GQ2H24MFR-T2C	128MX16(64MX32)	HPMH-14-00300000002G
SAMSUNG K4G10325FE-HC04	64MX16(32MX32)	HPMH-14-00300000003G
SAMSUNG K4G20325FC-HC04	128MX16(64MX32)	HPMH-14-00300000004G
Elpida EDW1032BABG-50-F	64MX16(32MX32)	HPMH-14-00300000005G
Elpida EDW2032BABG-50-F	128MX16(64MX32)	HPMH-14-00300000006G

For GDDR5: $0.7 \cdot VDDR1$

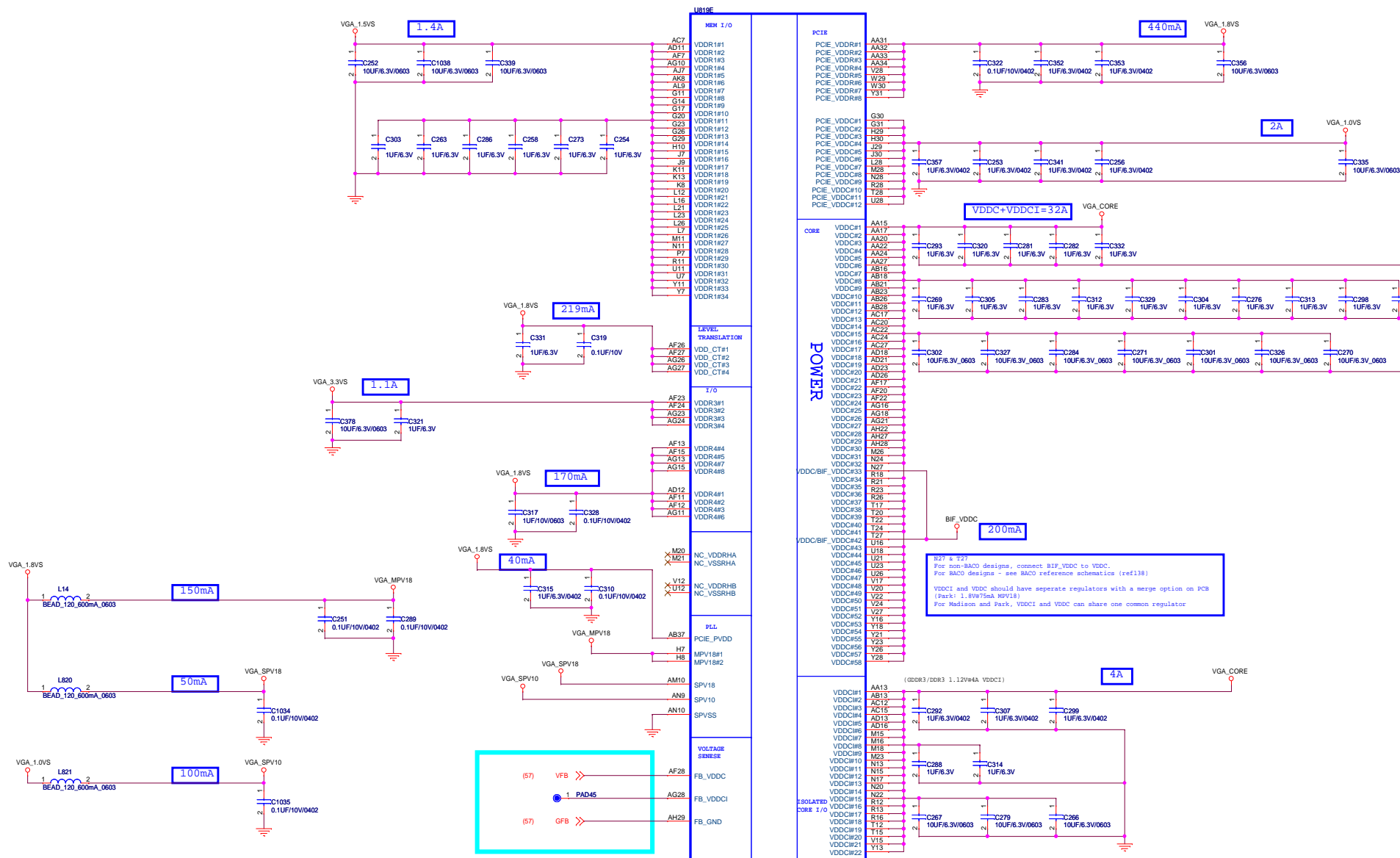


For GDDR5: $0.7 \cdot VDDR1$



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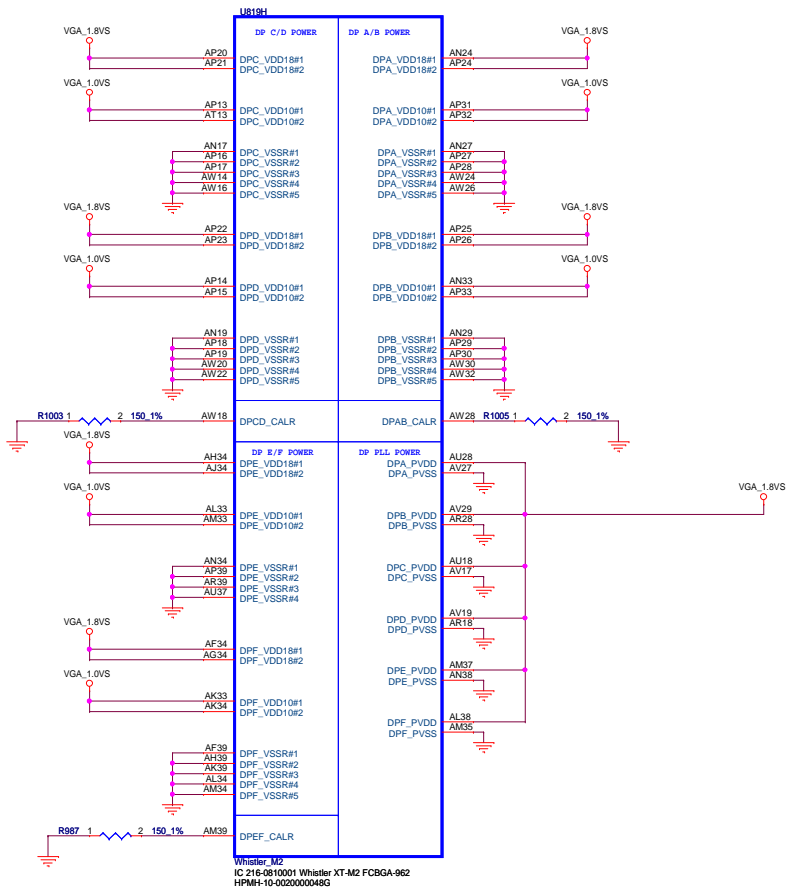


Whisper_M2
IC 216-0810001 Whisper XT-M2 FCBA-962
HPMH-10-0020000048G

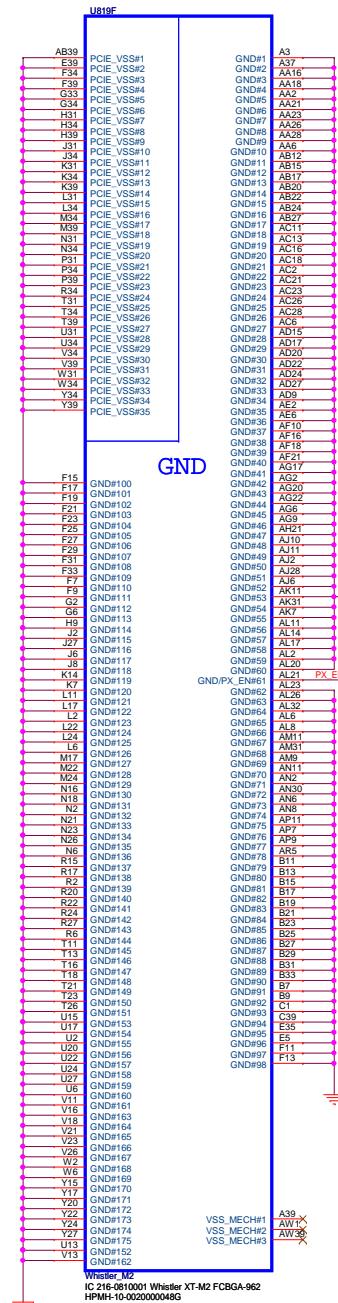
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Project
H71
Size:
Date:

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Whistler_M2
IC 216-0810001 Whistler XT-M2 FC8GA-962
HPMH-10-0020000048G



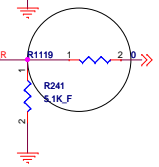
GND

BACO design options
See Apps Note
Seymour/Whistler
/Robson Supported
Park/Madison
Capilano/Broadway
Not Applicable

For PX_EN,
refer to the BACO
reference schematics
for detail

PX_EN is used to
control discrete GPU
regulators for
PowerXpress
(Switchable graphics)
BACO mode.

A pull-down resistor
is required.
Leave signal
unconnected
if not used.



PX_EN R1119 1 2 0 0 R241 1K F PX_EN (56.57)

VSS_MECH#1 A39
VSS_MECH#2 AW36
VSS_MECH#3 X

Whistler_M2
IC 216-0810001 Whistler XT-M2 FC8GA-962
HPMH-10-0020000048G

FLEX Computing

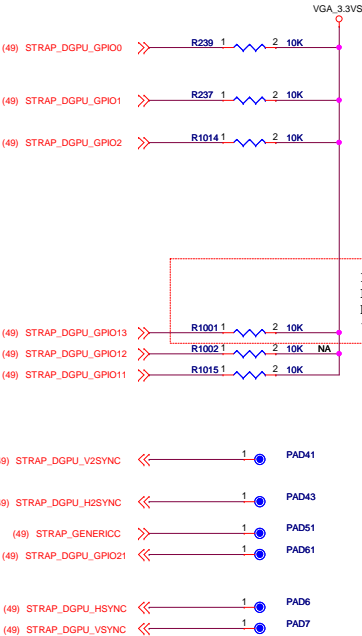
Project Name :	H710D11
Size :	Document Number : HPMH-10-0020000048G
Date :	Monday, November 1, 2010

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Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33 AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK: (3.3V) Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V) Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred but not required. SwaplockA/B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB - see above On a multi-gpu design,SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms) . If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output- on S3 package

CONFIGURATION STRAPS				
STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable. 0: 50% Tx output swing 1: Full Tx output swing (DEFAULT)	0 Internal Pull Down	Mounted
TX_DEEMPH_EN	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (DEFAULT)		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable 1 : PCIe device as 5.0 GT/s capable (DEFAULT)		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA NA
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable the external BIOS ROM device: 0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		Mounted
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 (DEFAULT) 64 MB 010 32 MB 011		Mounted NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RESERVED RESERVED RESERVED RESERVED	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function (DEFAULT) 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI if dongle is detected 1 1 Audio for both DisplayPort and HDMI		NA NA



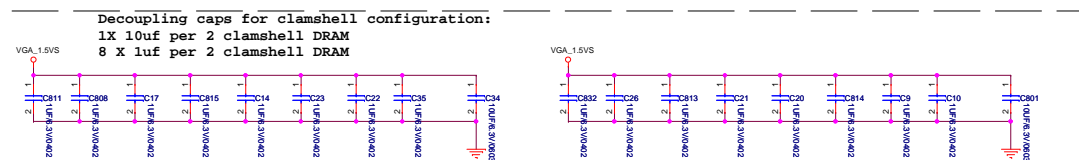
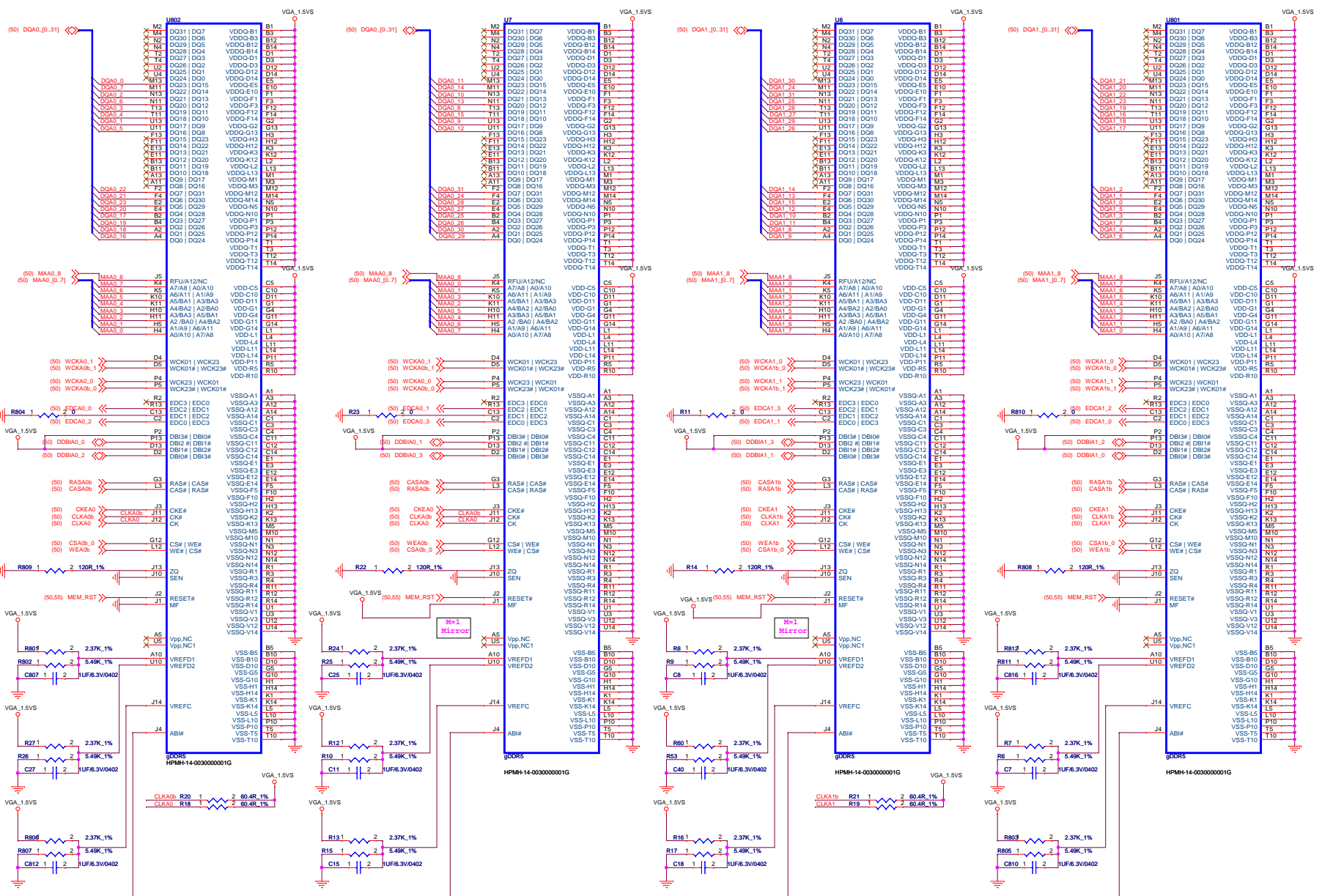
GPIO 13,12,11 CONFIG[2:0]
=>101 for PM25LV010

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Project Name: 4740D14 Title: Capilano STRAPS/ChioDiff

Size: Det

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NA for Seymour

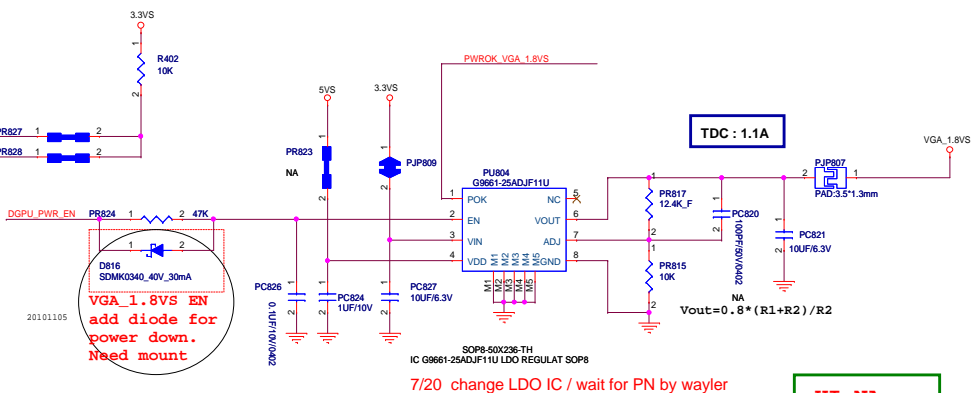
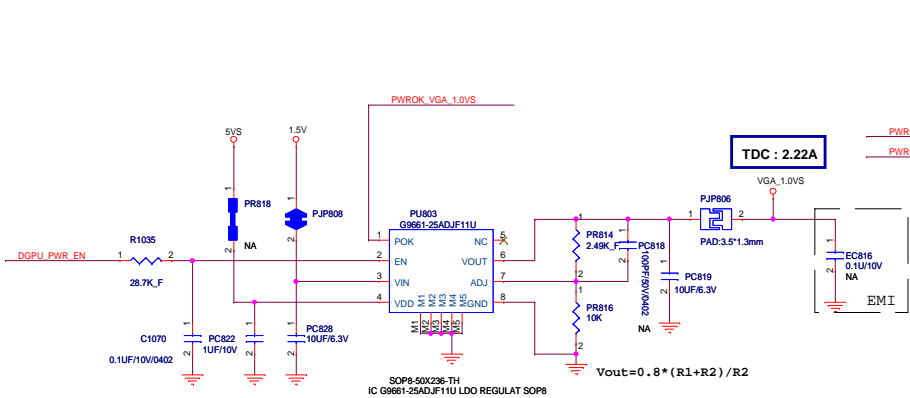
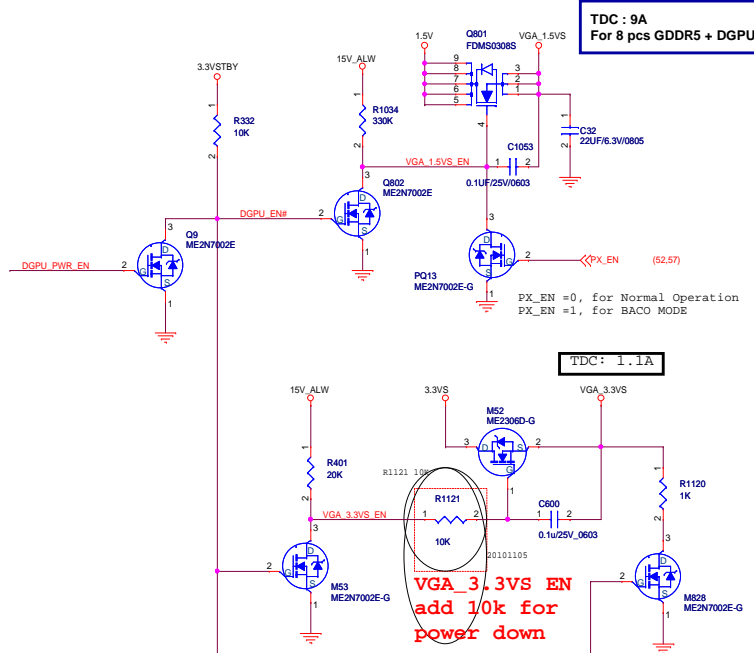
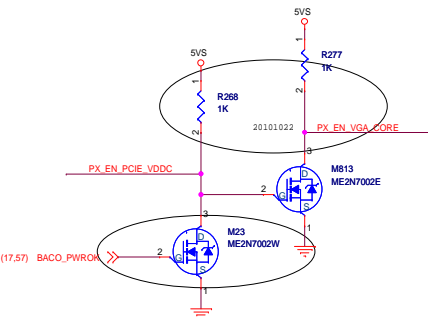
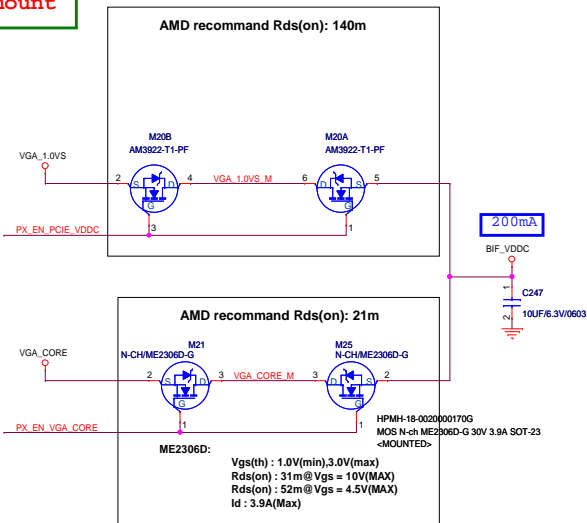
DDR5 Memory Channel A X16 Mode

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Project Name:	H710D1H
Document Number:	Caplan_VRAM GDDR5 64MX16 A
Size:	HPM14-40GB600-B130
Date:	Monday, November 08, 2010
Sheet:	54 of 63

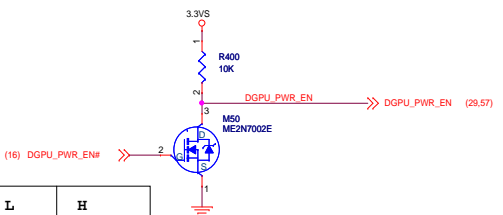
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UI NA
DI Mount

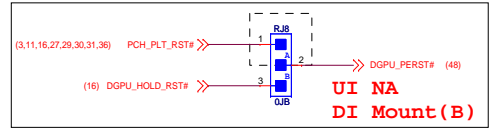
TDC : 9A
For 8 pcs GDDR5 + DGPU



UI NA
DI Mount



L	H
DGPU ON	DGPU OFF



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Project Name : H710DI1		T
Size :	Document Number : HPMH-4	
Date: Monday, November		

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VID4 (PP2) (GPIO16)	VID3 (PP1) (GPIO20)	VID2 (PP0) (GPIO15)	VGA_CORE
0	0	1	1.05V
1	0	0	0.900V

VID							V _{DAC} (V)
6	5	4	3	2	1	0	
0	1	0	0	1	0	0	1.0500
0	1	1	0	0	0	0	0.9000

5VS PU maybe leakage in BACO. Change to VGA_3.3VS

(49) PWRPLAY_VID2
(49) PWRPLAY_VID1
(49) PWRPLAY_VID0

VGA_CORE EN change R and C for power down

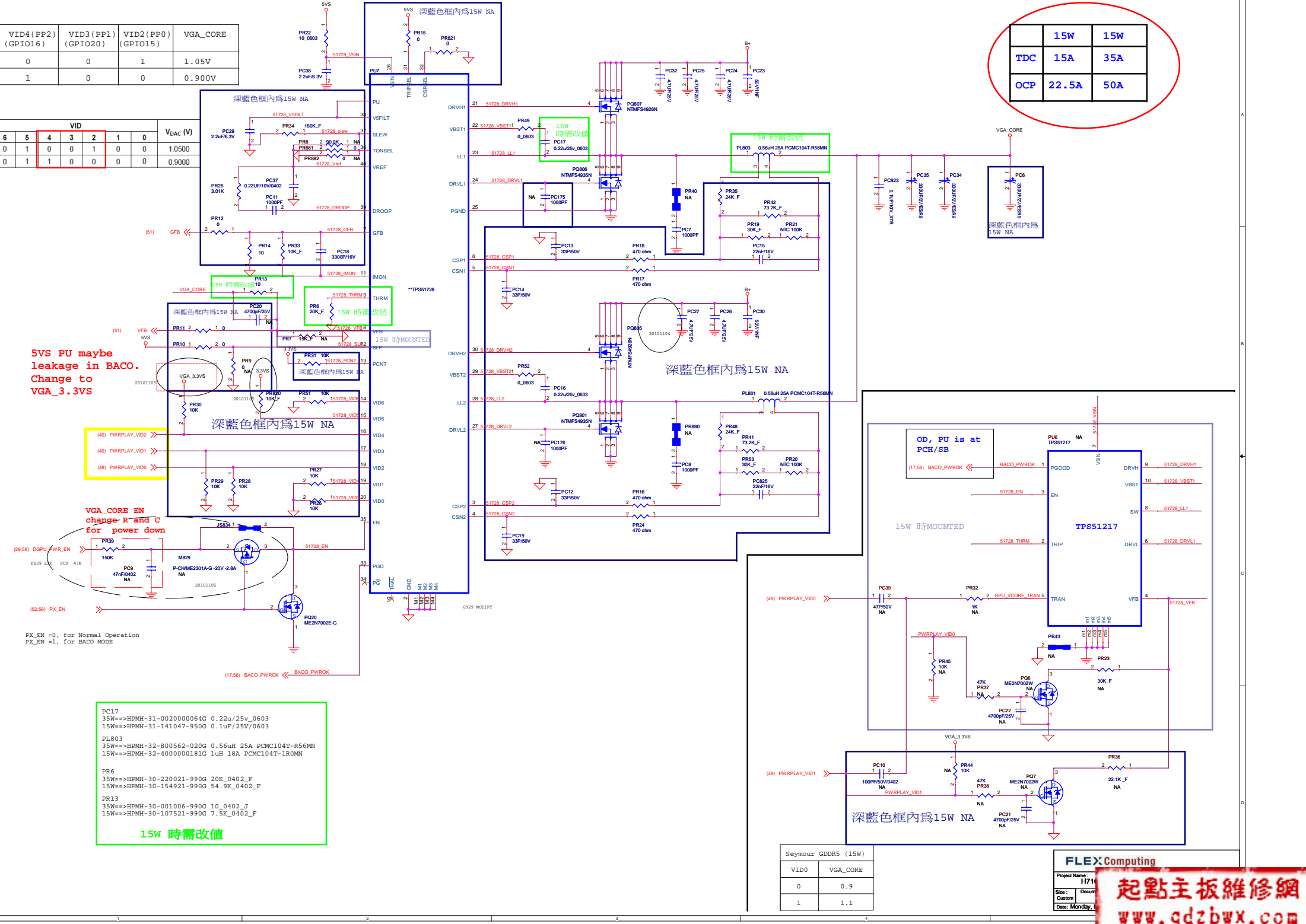
(29.56) DGPU_PWR_EN

(52.56) PX_EN

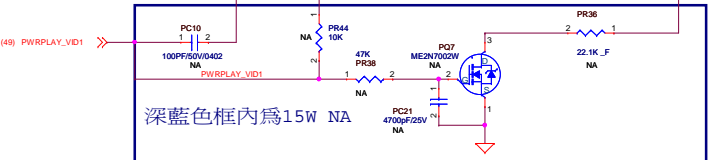
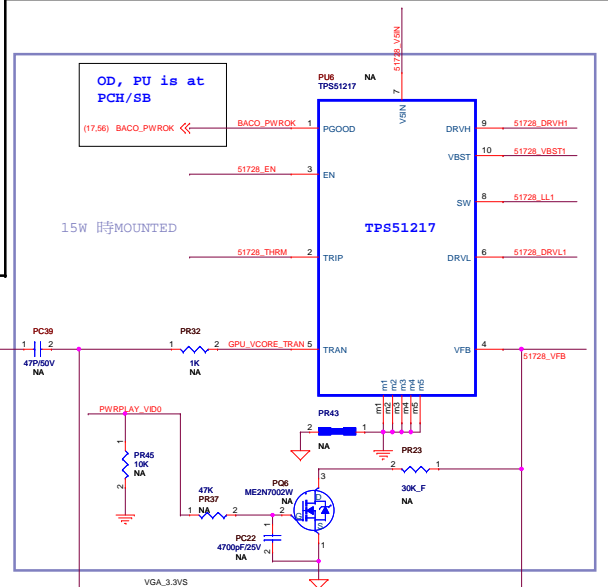
PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

PC17
35W==>HIPMH-31-0020000064G 0.22u/25v_0603
15W==>HIPMH-31-141047-950G 0.1uF/25V/0603
PL803
35W==>HIPMH-32-800562-020G 0.56uH 25A PCMC104T-R56MN
15W==>HIPMH-32-4000000181G 1uH 18A PCMC104T-1R0MN
PR6
35W==>HIPMH-30-220021-990G 20K_0402_F
15W==>HIPMH-30-154921-990G 54.9K_0402_F
PR13
35W==>HIPMH-30-001006-990G 10_0402_J
15W==>HIPMH-30-107521-990G 7.5K_0402_F

15W 時需改值



	15W	15W
TDC	15A	35A
OCF	22.5A	50A



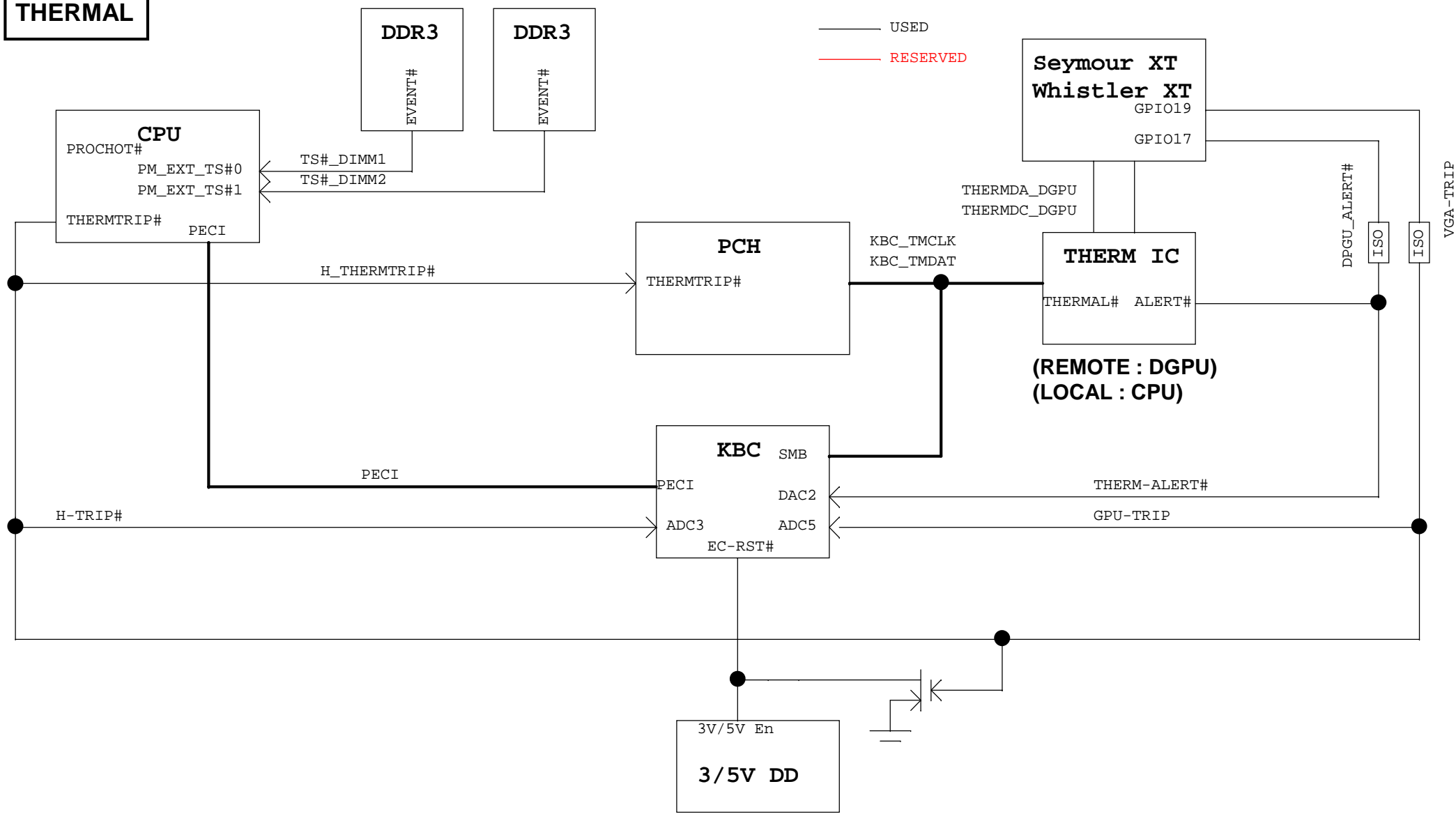
Seymour GDDR5 (15W)	
VID0	VGA_CORE
0	0.9
1	1.1

FLEX Computing

Project Name: H710
Size: Custom
Date: Monday, 1/1/2020

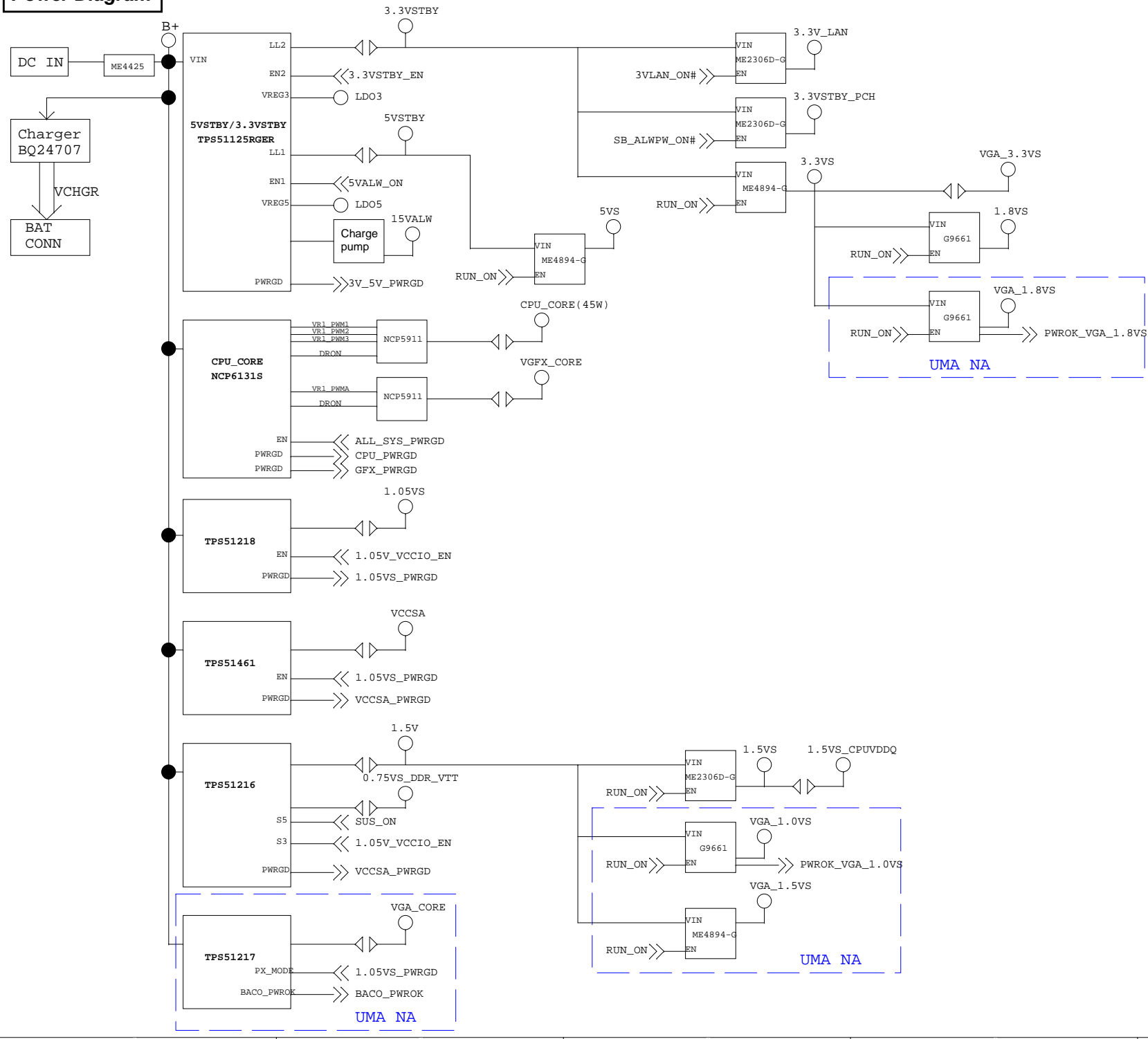
起點主板維修網
www.qdzbxw.com

THERMAL

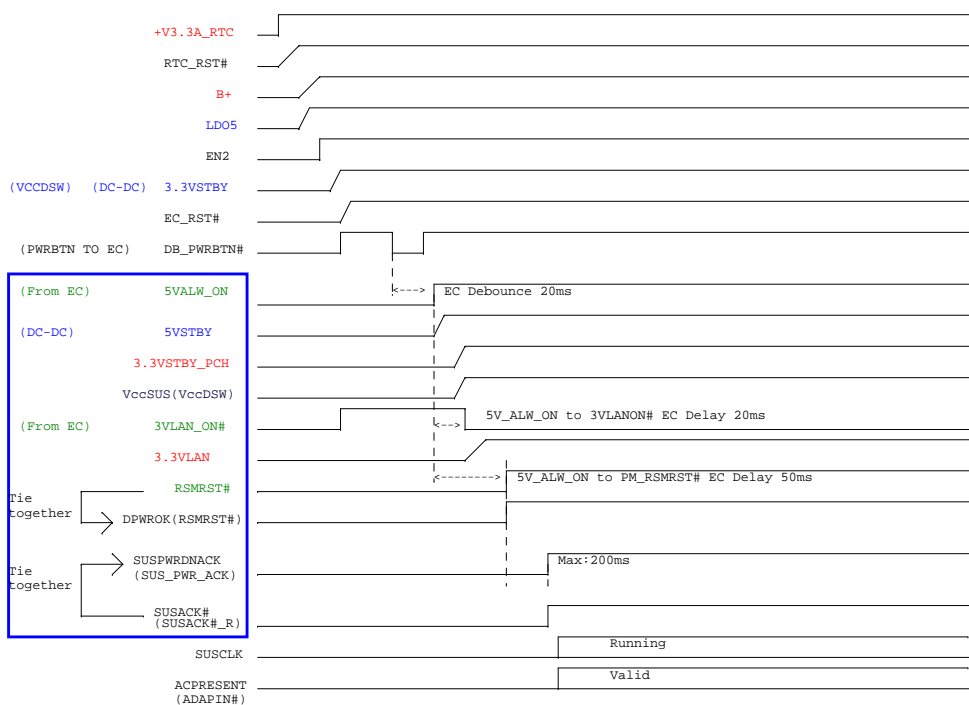


FLEX Computing			
Project Name : H710D11		Title : Thermal Policy	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet :	59 of 63

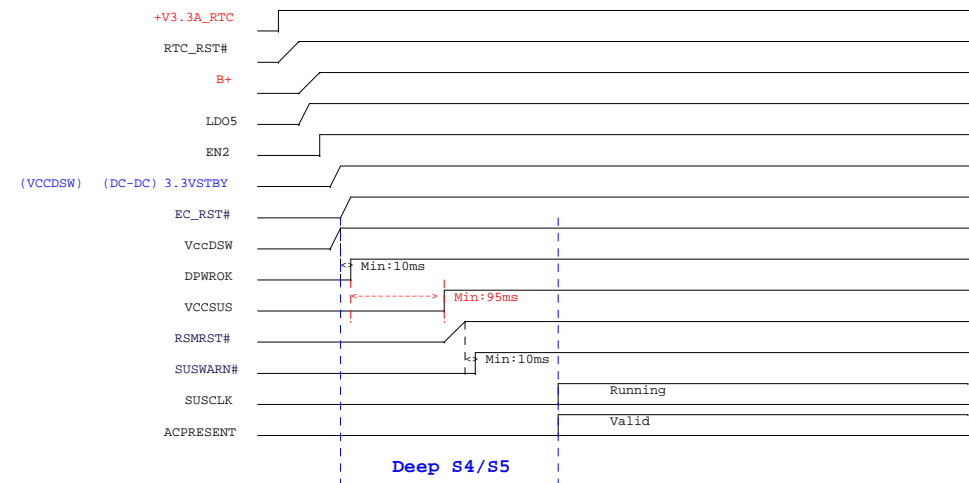
Power Diagram



G3 to S0 (without Deep S4/S5)

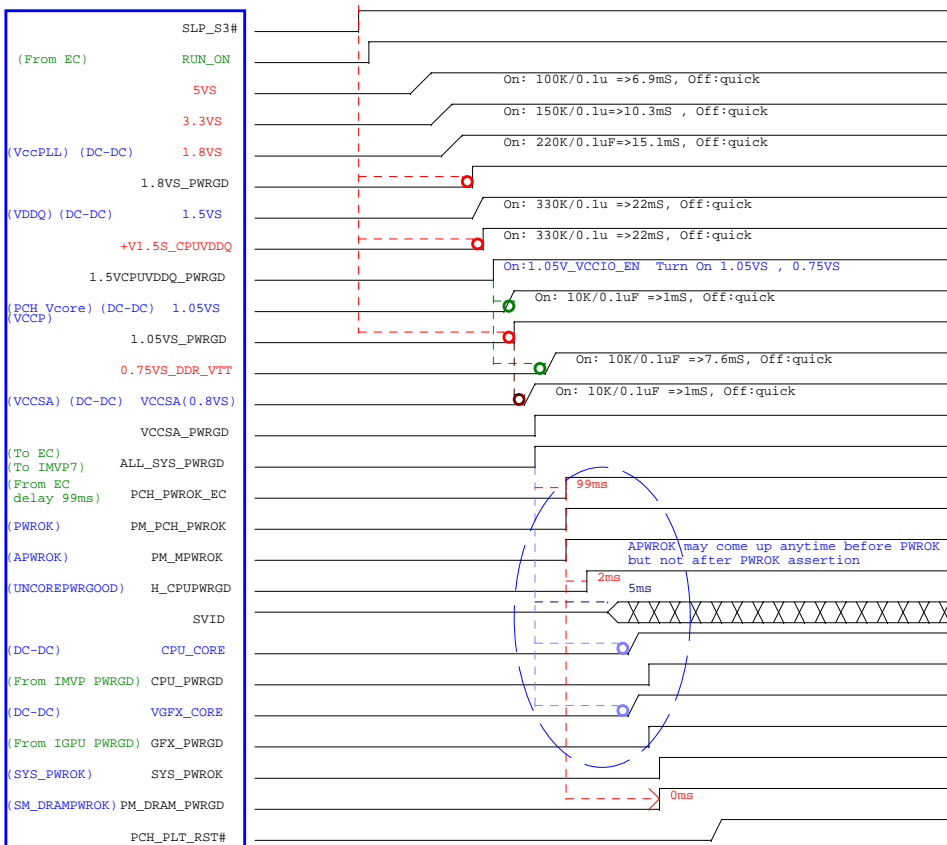
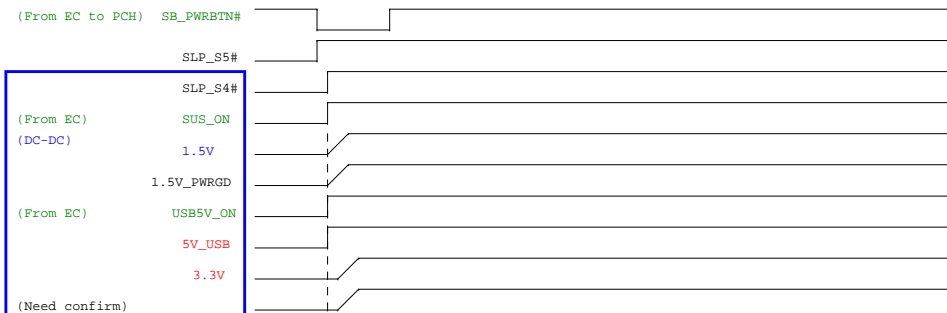


G3 to Sx (support Deep S4/S5) This Platform Without SUPPORT



Deep S4/S5

S5 to S0



Blue: PWM
Green: EC
RED: MOSFET or Others

S0 to S5 (WoLAN Disable) (without Deep S4/S5)

Signals shown:

- +V3.3A_RTC
- RTC_RST#
- B+
- +V5A_LDO
- EN2
- (VCCDSW) (DC-DC) +V3.3A
- EC_RST#
- (PWRBTN TO EC) PWRBTN#
- (From EC) 5V_ALW_ON
- (DC-DC) +V5A
- +V3.3A_PCH
- VCCDSW
- (From EC) 3VLANON#
- +V3.3A_LAN
- PM_RSMRST#
- DPWROK
- SUSPWRDNACK (SUS_PWR_ACK)
- SUSACK# (SUSACK#_R)
- SUSCLK
- ACPRESENT

Timing annotations:

- RSMRST# Low to 5V_ALW_ON Low (EC delay 10ms)
- RSMRST# Low to 3VLANON# High (EC delay 2ms)
- Tp (SLP_S3# Low to RSMRST# Low) > 500us

States:

- SUSCLK: Running
- ACPRESENT: Valid

S0 to S5 (support Deep S4/S5)

Signals shown:

- +V3.3A_RTC
- RTC_RST#
- B+
- +V5A_LDO
- EN2
- (VCCDSW) (DC-DC) +V3.3A
- EC_RST#
- VCCDSW
- DPWROK
- SLP_SUS#
- VCCSUS
- PM_RSMRST#
- SUSACK#
- SUSWARN#
- SUSCLK
- ACPRESENT

States shown:

- Running
- Valid

Deep S4/S5

RED: MOSFET or Others

[illegible]

Start Shutdown Sequence

